

Appendix J

DEVICE PHYSICS

Using basic physics to extract model parameters for modeling and simulation

Abstract: TCAD modeling tools are used to extract circuit model properties for SPICE from the structure, material, and electrical properties of semiconductors. Device design determines electrical performance. TCAD provides a link between semiconductor device design and the electrical behavior represented by models for those devices. Throughout this chapter, discrete semiconductors are used as examples in the discussion of the link between device design and model parameters.

J.1 INTRODUCTION

Simulators are wonderful, almost magical tools. But if simulators get inappropriate model parameters, they produce garbage—*not* useful answers. To ensure that useful output is generated, engineers need knowledge, understanding, and insight to help them avoid making mistakes. The authors recognize that understanding basic concepts and where the numbers come from are important in appreciating the simulation results. This chapter provides insight into semiconductor modeling for those engineers interested in these matters.

This appendix contains more detail than “Chapter 3, Model Properties Derived from Device Physics Theory.” Together, chapters 3, 4, and 5 cover fundamental knowledge that will help users avoid making mistakes in modeling and simulation.

J.2 WHY MODELING DEEP SUB-MICRON TECHNOLOGY IS COMPLEX

CMOS models and equations (J-23) to (J-27) emphasize modeling from a physical perspective. These models are simpler and easier to follow than a full development for deep-sub-micron CMOS. There are currently about a dozen different high-level deep-sub-micron CMOS models, each involving over 70 parameters. Some models incorporate as many as 200 parameters. Most of these models and parameters are not totally portable from one simulation platform to another. Much of the modeling is proprietary and unavailable to the general public. Many of these models are based on UC-Berkeley models [117].

This topic is an overview of modeling methods. Therefore, what is the purpose of presenting CMOS models in full detail to an audience unlikely to specialize in model extraction? The answer is that the authors want circuit designers to understand the physical basis of SPICE models.

For today's deep-sub-micron IC lateral MOSFET devices, modeling assumption require the realization that horizontal spacing comparable to vertical spacing. The horizontal BJT formed as part of a MOSFET in a substrate well becomes available as a significant circuit element. This BJT can be used as a low-gain element in a design. The opposite side of this convenience occurs when the BJT shows up as an unwanted parasitic element.

For deep sub-micron CMOS, higher-order effects that were negligible have become significant, to the point of sometimes dominating over the first-order effects. In the early days of SPICE modeling, it was assumed that most of the current flow was across a flat area, and that the effects of perimeters and corners could be neglected. For instance, sidewall capacitance is insignificant in a large-area discrete (vertical) BJT. But it predominates other capacitances in a deep sub-micron lateral IC BJT transistor. Later models added some perimeter effects.

A typical fine emitter finger on a 2N3904 (or a 2N918 RF transistor), developed in the early 1950s, might be a mil or two (25 to 50 microns) across. Today's advanced IC technology is working with geometry features below 0.1 micron. The modeling of today's integrated circuit BJTs and MOSFETs is a whole new situation from when SPICE was first developed

By today's standards, the small signal 10x15 mils to 30x30 mils discrete device described in "Chapter 7, Using Data Sheets to Compare and Contrast Components" may seem huge. However, consider some high-power giant BJT transistors that were being sold in the 1970s. Such devices sometimes took an entire 3½-inch diameter wafer per device (the largest wafer then in common use). Today wafer diameters are at 12 inches and larger. We still

use power transistors of similar size to handle high-power and high-current. Small-signal transistors remain in use as well, typically offered in 1/8 W to 1 W packages. For comparison, today's integrated circuit transistors are made in CMOS, with each transistor handling around 50 micro Watts.

Figure J-1 shows a single transistor, n-channel, packaged, Insulated Gate Bipolar Transistor (IGBT), the MG300Q1US51. This component is currently sold by Toshiba Semiconductors. The package is about 10 x 6 x 2.5 centimeters. The device handles 300 A, 1200 V, and 2500 W.

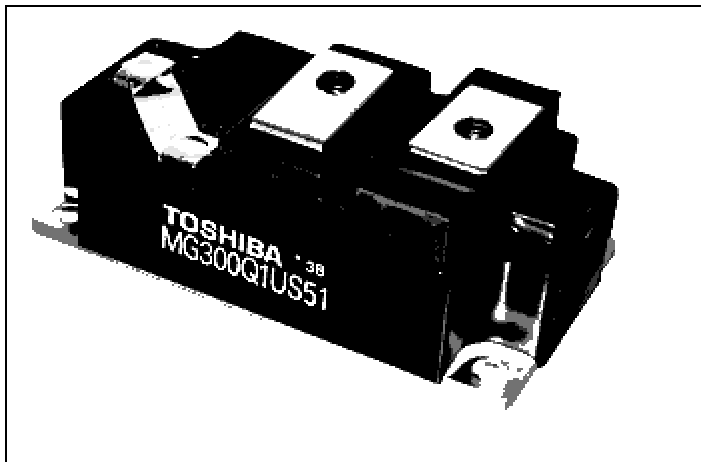


Figure J-1. A high-power silicon IGBT from Toshiba Semiconductor

A 10x15 mil device occupied 150 mils² of wafer. A 3½-inch wafer provides 9,621,127 mils² of surface. That is an area ratio of 64,140 times larger for the giant transistor than our 40V, 200mA small signal ½-watt device. The giant power BJT is able to handle 100V, 100A, and 243 watts. There are also power devices handling 150V, 200A, and 3000 watts.

J.3 MODELS EXTRACTED FROM SEMICONDUCTOR DESIGN THEORY

One way to model a semiconductor device is to extract its model properties from the device's structure and materials physics. When we take this model extraction approach, it is possible to model a device without ever building it.¹

¹ This is parallel to modeling and simulating a circuit on a computer before prototyping it.

There are important advantages to being able to extract model properties from theory. One advantage is being able to develop models on new devices while concurrently designing a new PCB. Another advantage is being able to develop model parameter distributions. These simulated distributions represent the predicted variability of a device's population. They can be generated very early in the device's life cycle.

Often usage rates and the amount of product produced are small. Therefore, gathering significant population statistics from measured units is not possible. But with simulation we can still predict the likely *range* of product variation. This predicted range can be used in simulating a circuit.

The computer aided engineering programs that provide the ability to extract SPICE device models from semiconductor structure and physics are generically called (semiconductor) Technology Computer Aided Design (TCAD) programs.² These TCAD programs also aid semiconductor device design engineers and process engineers to design the structure, materials, and processing that yield the desired electrical properties.

In this chapter, we use Bipolar Junction Transistor (BJT) technology to explain how structure determines performance. We also use it to show the interrelationship between many modeling ideas. In the past, BJT technology was a major player, but today it is only a niche player.³ However, BJT technology is still likely to be familiar to most readers so it makes a good starting point in our discussions. The BJT device and circuit models are used to introduce some device physics and modeling concepts. BJTs are also relevant to those working with BiCMOS circuits.

Deep submicron CMOS FETs have parasitic BJT action, so understanding some basic BJT operation is necessary. Indeed, nearly all FETs can potentially have a parasitic BJT associated with their structure. And nearly all BJTs can potentially have a parasitic surface inversion FET associated with their structure. When the transistor was first invented, its inventors were looking for surface inversion transistor action, instead they found a parasitic BJT and recognized that it was a new type of transistor.⁴

In summary, if we want to understand and use device physics to our advantage, we need to understand some BJT behavior, which is a good starting point for explaining semiconductors.

CMOS technology has taken over most applications, even differential signaling. But with today's sub-sub-micron technologies, deep submicron CMOS is far more complex to explain. The author's purpose is to illustrate

² References to read are [11, 32, 33, 117, 140].

³ For readers interested in learning more about current CMOS technology, see [11, 40, 77, 127, 140].

⁴ The high level of surface ionic contaminants, due to the semiconductor processing of the day, masked the surface inversion action they were looking for.

some relationships between device structure and model properties. It is important to understand that the relationships both enable and limit device behavior.

J.4 EXAMPLE OF SEMICONDUCTOR PROCESS TECHNOLOGY TO CONSTRUCT A BJT

Semiconductor device modeling starts with semiconductor device design. Process technology determines device design. Throughout this chapter, the authors use as an example a discrete BJT, which uses planar epitaxial double-diffused technology.

A crystal ingot of semiconductor material (typically silicon but not exclusively) is grown and sliced into thin wafers that will serve as a substrate for semiconductor devices. A pure silicon crystal is a semiconductor but not a very good one. Dopant atoms are added to it to alter its properties in a controlled way in particular regions of the crystal.

Typical dopant atoms are phosphorus for n-material and boron for p-material. phosphorus has five electrons in its outermost atomic electron shell. Thus it easily contributes a conduction electron when thermally excited. Boron has three electrons in its outermost atomic electron shell. Thus it easily accepts a conduction electron when a thermally excited. The electron is contributed from a neighbor atom, usually silicon. Another way of saying this is that p-dopants contribute a “hole” to the crystal lattice. The conduction electrons and holes migrate more easily through the crystal lattice under the influence of concentration gradients (diffusion) and electric fields built-in by structure or applied as external bias.

The dopant atoms substitute for and replace silicon atoms in the crystal structure. At very low dopant concentrations we still have a low conductivity material much like pure silicon. At very high dopant concentrations we have a high conductivity material that behaves electrically more like a metal conductor. Dopant atoms are not the same size as silicon atoms that they replace in the crystal structure. Thus, each dopant atom strains and distorts the crystal lattice slightly.

One objective is to get the dopant concentrations just right. Dopant concentrations are hard to get exactly right during crystal growth. So, the substrate is usually doped heavily n or p. The substrate then serves as a crystal matrix upon which additional crystal material can be grown. An epitaxial (epi means grown upon) layer is often grown on the crystal substrate by gas vapor deposition. Dopant concentrations and epi layer thickness can be tightly controlled. The epi layer repeats and extends the

substrate's crystal structure. Low dopant concentrations of the same dopant type as the substrate are normally used.

Silicon easily forms an oxide layer, SiO_2 (rusts) on its surface when exposed to air. This is fortunate. The SiO_2 layer is strong, and impervious to contaminants (and dopants). The silicon surface thus has the important property of being self-masking. Unless we etch open a window in the oxide layer we cannot deposit dopant atoms for diffusion into the silicon. Ion implantation of dopant from a plasma source can be done through a thin layer of oxide with more precision.

Thus far we have created a $n^+ - n^-$ — oxide layer cake structure that is potentially the collector and backside contact of our BJT. The SiO_2 can be etched open for the precise placement, deposition, implantation, and diffusion of additional dopants to further create the device structure.

Figure J-2 shows a typical net dopant concentration profile for a pnp example though our vertical BJT from (topside) emitter-to-base-to-collector (backside). x is distance in from the topside in microns. An npn example would look just the same with material polarities reversed from the pnp example. Figure J-3 is a simplified view of some of the process steps.

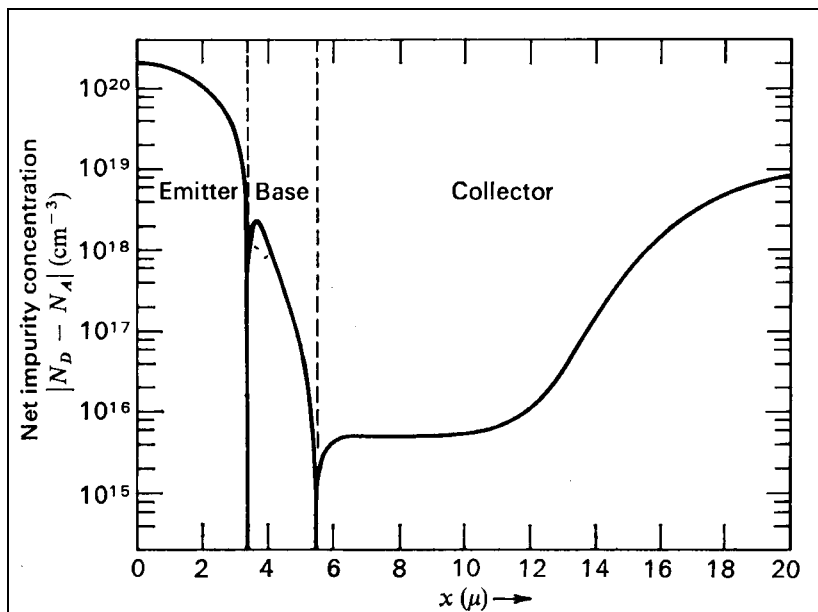


Figure J-2. Net dopant distribution: pnp example [38] p225

Let us next look at the process construction steps in individual device cell. In this example these steps will form the base region first, and then the

emitter region. The two steps are called double-diffusion because heat/concentration driven diffusion is used to *drive-in* the chemical dopants used to form our base and emitter regions. The junctions between the p materials form the location of the emitter, base, and collector regions. The dopant gradient, net dopant concentrations, and junction depths determine many important electrical properties of the finished device.

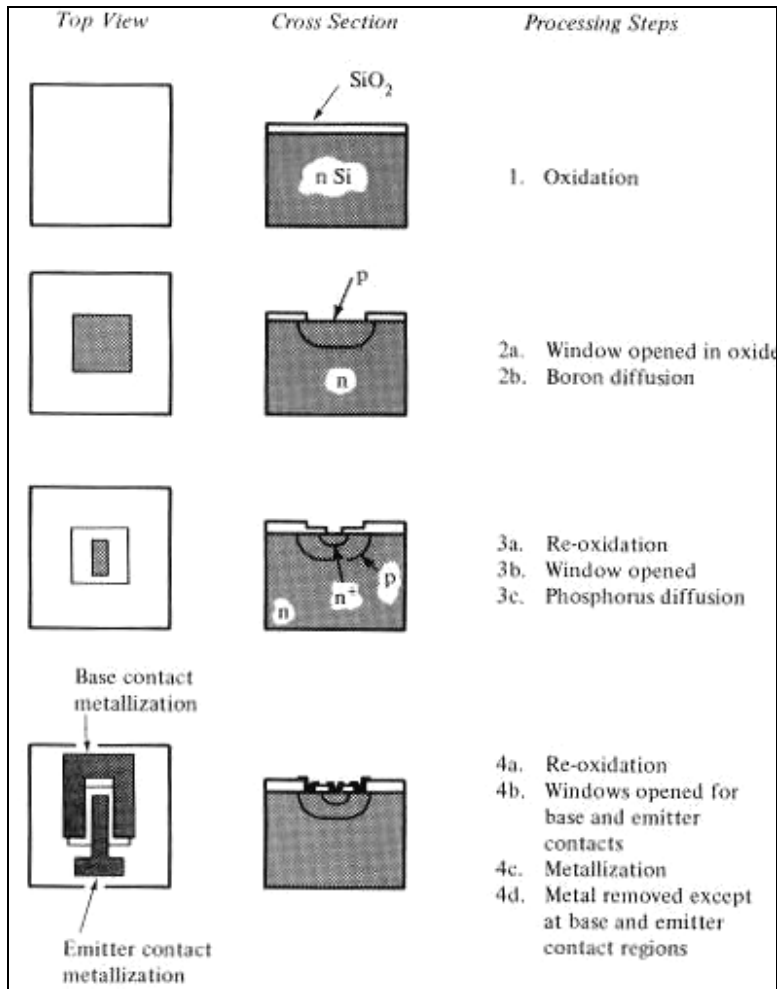


Figure J-3. Steps in fabricating an npn transistor by double-diffusion of boron and phosphorus in an n-type Si substrate [118 p240]

The diffusion of chemical atoms is infinitely slow at temperatures we are likely (perhaps up to 250 deg C) to encounter. The drive-in diffusion is done at temperatures like 900 deg C to perhaps 1200 deg C. At 1400 deg C the silicon becomes plastic and begins to flow. The diffusion of the chemical elements is similar to the diffusion of electrons and holes, both being driven by concentration gradient and thermal energy. Electron (hole) diffusion at room temperature is significant while dopant atom diffusion is insignificant.

Figure J-3 shows the processing steps for a discrete npn BJT device in very simplified format. First a window is opened in the SiO_2 layer for depositing/implanting enough boron to change over our n- region to a net p dopant concentration. Then, during drive-in and re-oxidation the window is closed with a fresh layer of SiO_2 . Next, a window is opened on top of our p region and enough phosphorus is deposited and driven in to change the net dopant concentration back to n-material for our emitter.

In an actual process we would create many identical devices on our layer-cake structure using printing lithography through a set of process masks and steps and/or step-and repeat printing. At the end of the process individual devices (chips) would be separated from each other by scribing and cracking them apart. The silicon wafer retains many of the mechanical properties of a crystalline ceramic and will fracture into individual devices along scribe lines like a piece of window glass.

The upper half of Figure J-4 shows a cross section through a vertical BJT npn device. The lower half shows an idealized one-dimensional model of the device. We refer to this one-dimensional model later in this chapter.

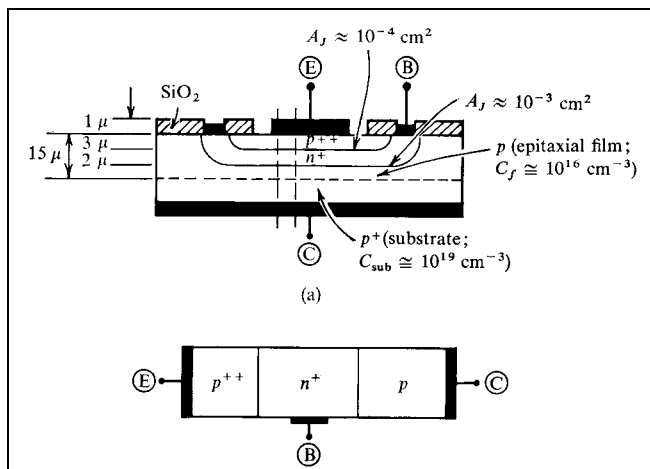


Figure J-4. Vertical BJT cross section [47]

Legend:

E=Emitter

B=Base

C=Collector

J.5 HOW BJT AND FET CONSTRUCTION AFFECT THEIR OPERATION

J.5.1 BJT Construction and Operation

A BJT (bipolar junction transistor) is a device with a p-n (or n-p) semiconductor junction similar to that found in a diode. When the junction is forward-biased, it *emits* (injects) current carriers from one side of the junction to the other. This effect is usually enhanced by the doping concentration profile of the junction and base region. The injecting (emitter) side usually has a much higher doping concentration than the receiving side. The region into which the current carriers get injected is called the *base*.

On the other side of the base region is another semiconductor junction, n-p to correspond with p-n (or p-n to correspond with n-p). This junction is reverse biased (V_{cb}). Current carriers are normally not injected into the base region from it. This effect is usually enhanced by the doping concentration profile of the junction. The base region usually has a much lower doping concentration than both the emitter and collector regions.

This p-n-p (or n-p-n) arrangement is similar to bringing two forward facing diodes together, pointing at each other in a series connection. This arrangement is not very exciting because the injected carriers tend to recombine in the base region before they get very far.

Figure J-5 shows an energy band diagram scanning across our BJT from and to emitter-base-collector.

- E_c = conduction band energy level
- E_f = Fermi energy level
- E_v = valence band energy level

The top part of Figure J-5 shows the energy band diagram without externally applied bias voltage. The bottom part of Figure J-5 shows the energy-band diagram with externally applied bias voltage. Forward bias applied emitter-base lowers that energy band and enhances the injection of current carriers into the base. Reverse bias applied collector-base raises that energy band and discourages the injection of current carriers into the base.

An n-emitter injects electrons into a p-base. A p-emitter injects holes into an n-base.

What happens when the base region is made so narrow that some carriers arrive at the reverse-biased junction? The minority carriers have arrived on the wrong side of a reverse-biased junction and the electric field attracts them across the junction into the collector. The junction is still reverse-biased to carriers on the collector side. But it is forward-biased to carriers of the same polarity on the base side. Carriers of that polarity would normally not be there had they not been injected from the emitter and then diffused across the base.

The result is that the carriers get swept up, or *collected*, into the p (or n) region. Conduction from the emitting-to-collecting region can be controlled with a low-voltage, low-energy, and low-impedance emitter-base circuit. Large currents can be made to flow in a higher-voltage, higher-energy, higher-impedance base-collector circuit. This is an interesting and useful result. Many applications take advantage of the current, voltage, and power gains in a bipolar transistor.

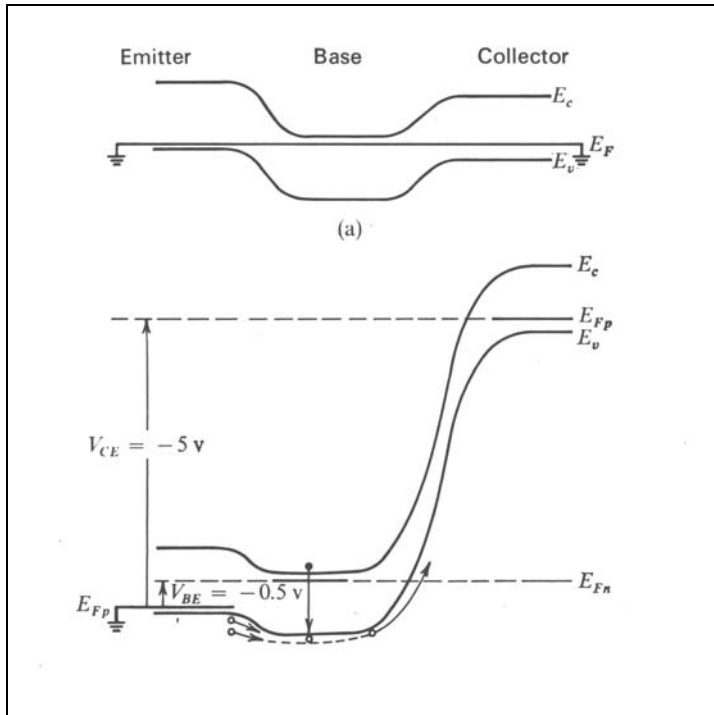


Figure J-5. Energy band diagram for a pnp BJT transistor [47]

Minority current carriers that do recombine in the base (fall out of the conduction or valence band) and re-attach at a particular atomic site would cause a net, imbalanced charge, un-neutralized at the atomic level to build up in the base. When the current carrier is a conduction-band electron (hole) that loses energy and re-attaches to the semiconductor lattice, it does so at the site of an atom with a hole (electron) that can accept it. Before that event, the atom is electrically neutral. That is, the electric charge of the nucleus is balanced by the charge of the electrons in shells around it. When the extra electron (hole) injected from the emitter attaches to the atom, it unbalances the charge on the atom.

In essence, unless we supplied the means to drain off the extra charges in the base via base current, the accumulated extra charges would quickly repel any further injection from the emitter. The base current that we must supply, I_b , represents the inefficiency of conducting carriers across the base region. The view of a BJT as a *current gain* device can be a bit misleading. It is the built-in junction voltages (due to the energy band and modifying effects of temperature and dopants), plus the applied external voltage biases across those junctions that control injection and collection of carriers across the base. Base current does not get multiplied and flow out of the collector.

Figure J-6 is a simplified one-dimensional model of the BJT that can be applied to understanding both vertical and lateral (IC) implementations:

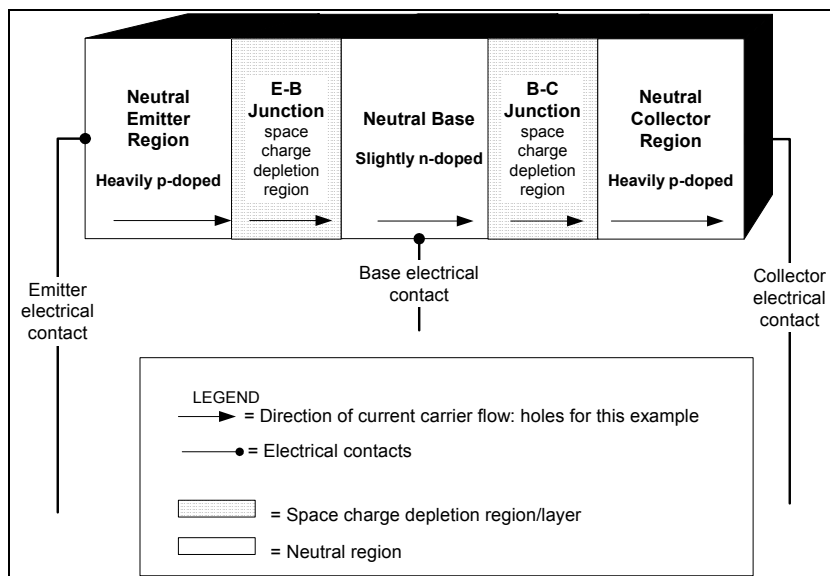


Figure J-6. A one-dimensional structural model of a pnp transistor

Figure J-7 represents the construction of a *lateral* BJT done as part of an integrated circuit (IC). Here, each device is isolated from its neighbors and the backside substrate by sitting in a well formed by *isolation diffusions*. Contact to the buried collector is done through the topside of the IC — collector metal-contact⁵ to (collector) contact-diffusion to buried-collector.

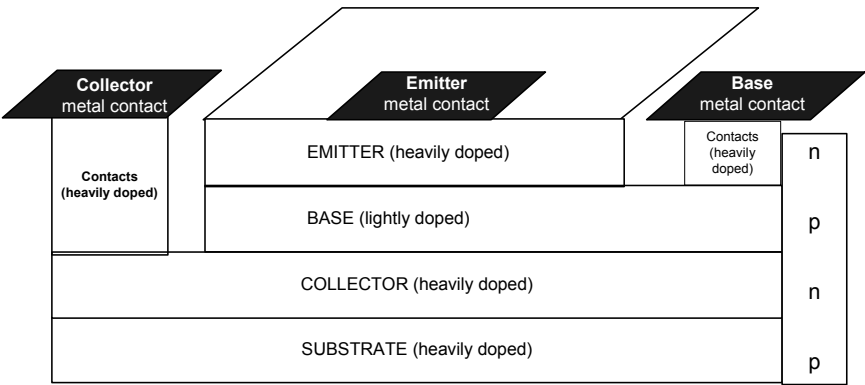


Figure J-7. Typical lateral BJT construction for an individual transistor

J.5.2 Two Types of FET

The BJT is a semiconductor device dominated by minority current carrier and p-n/n-p junction effects. A Field Effect Transistor (FET) is a semiconductor device dominated by majority current carrier and channel conductance effects. A FET can be constructed in two forms:

- The Junction FET (JFET) transistor. Channel conductance is controlled by space-charge depletion layer changes.
- The Metal-Oxide-Semiconductor (MOSFET) transistor. Channel conductance is controlled by surface-inversion layer changes.

The MOSFET contact pads and field plate can be implemented in metal or in heavily doped polysilicon (semicrystalline silicon). In today’s CMOS chips, the field plate is always implemented in polysilicon.

⁵ Throughout the book, metal to die contacts are usually non-rectifying, non-Schottky Barrier diode contacts.

J.5.3 JFET Construction and Operation

JFETs are interesting and useful devices. They are interesting because they illustrate certain space-charge layer aspects of semiconductor behavior. However, JFETs are even smaller niche players than BJTs.

In the JFET, a conduction *channel* of n or p material inside a semiconductor is controlled by the surrounding material (*gate*) of the opposite material polarity (p for n-channel, n for p-channel). Conduction from a *source* end to a *drain* end of the channel is established by imposing a voltage across the two ends. Source and drain are easily interchanged. The channel region is lightly doped, while the gate, source, and drain regions are more heavily doped.

The p-n (or n-p) junction formed under the gate is reverse biased and is used to control the channel conduction width by varying the width of the space-charge depletion region width. This is why the electrode attached to the surrounding channel width-control-region is called the *gate*. The gate is always reverse biased and thus supplies only leakage current. The leakage current is *much* (orders of magnitude) smaller than the base current.

J.5.4 MOSFET Construction and Operation

Modern MOSFET transistors are capable of performing nearly all switching and amplifier tasks and performing them better than alternative technologies such as BJTs. Deep submicron CMOS technology is certainly the technology of choice in high-speed logic and low-level RF amplifier circuits.

The MOSFET is constructed by placing a metal (or polysilicon) electrode over a lightly doped, semiconductor conduction channel; an insulating oxide layer separates them. This forms a layered Metal-Oxide-Semiconductor (MOS) structure at the surface of a semiconductor crystal. As with the JFET, the source and drain, located on opposite sides of the gate, are more heavily doped. Leakage current across the oxide is *much* (orders of magnitude) smaller than JFET leakage current. The DC bias current that needs to be supplied by the gate is negligible; the transient current is usually larger, due to the gate capacitance ($I(t) = C \cdot dV/dt$).

In Figure J-5, we see how an insulating oxide layer covers a surface channel. A metal field electrode called the *gate* sits over this oxide layer. The contact at one end of the conduction channel⁶ is made through a *source*; the contact at the other end of the channel is made through a *drain*. The

⁶ The channel does not exist when no gate bias is applied. It is initially a surface p-layer. Under the influence of a gate bias, the surface p-layer inverts to n-type, and a channel is formed.

source and drain are heavily doped n-regions.⁷ The conduction channel between them is a lightly doped p-region. In Figure J-9 we have the same construction in a complementary pnp device. In both cases, conduction from a *source* end to a *drain* end of the channel is established by imposing a voltage across the two ends. Source and drain are easily interchanged.

How does a MOSFET work? The answer depends on underlying construction, dopant concentrations applied during manufacture, and bias applied during operation. There are two possible modes of operation: *enhancement* mode and *depletion* mode.

J.5.4.1 Enhancement Mode MOSFET

Electrons generated by thermally excited dopant atoms are present in the heavily doped source and drain, but cannot flow through the normal enhancement mode p-channel between them with zero bias applied to the gate, and nothing else done to *invert* the surface. What does it mean to invert the surface and what is the result of such inversion?

Let us apply a positive gate voltage to our npn n-channel NMOS device. Holes will be repelled from the surface and electrons will be attracted to it. As we continue increasing the positive bias voltage, more of this migration of electrons occurs. At some point, the concentration of attracted electrons can become higher than the background concentration of holes supplied by the p material. For a thin layer near the silicon surface, the *apparent* character of the silicon goes from p to n. That is, it *inverts*.

Electrons can then carry current between the source and drain through this inversion layer. The value of V_{GS} at which enough mobile electrons are attracted to the surface region to invert it is called the *threshold voltage*, V_t . Removal of the bias voltage causes the character of the inversion layer to revert back to its original p character and conduction ceases.

In the inversion action just explained, a further increase in applied positive, gate bias voltage further *enhances* the conduction process. See Figure J-11 for the characteristic curves of an enhancement mode MOSFET.

For an enhancement mode p-channel pnp PMOS construction, the role of holes and electrons are swapped, and a negative gate voltage is used to create the inversion layer.

⁷ High conduction and low resistance. These regions are essentially contacts to the conduction channel.

J.5.4.2 Depletion Mode MOSFET

What does it mean if the surface is already inverted and what is the result of such inversion?⁸ In this case, the conduction channel already exists and current flows with zero gate bias applied, but source-to-drain bias applied. Such was the case for the discoverers of the BJT transistor. Surface contamination ions had already inverted the surface of their prototype device.

Let us apply a positive gate voltage to our npn n-channel NMOS device. More gate voltage increases the conduction just as before. Now, however, if we apply a negative gate voltage, we repel electrons from the conduction channel, the channel becomes shallower, and its conductivity decreases.

In the decreased conduction action just explained, an increase in applied negative gate bias voltage further *depletes* the conduction carriers. The value of V_{GS} at which enough mobile electrons are repelled out of the surface inversion channel to shut off all conduction—even with applied V_{DS} voltage—is called the *threshold voltage*, V_t . Removal of the gate bias voltage causes the character of the inversion layer to revert back to its original n character and conduction resumes.

For depletion mode p-channel pnp PMOS construction the role of holes and electrons are swapped, and a positive gate voltage is used to deplete the inversion layer. See Figure J-12 for the characteristic curves of a depletion mode MOSFET.

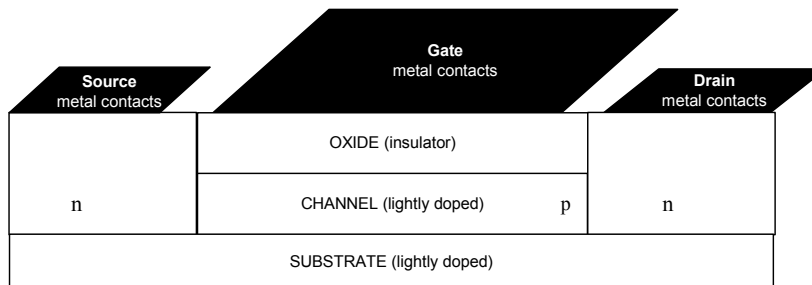


Figure J-8. Typical lateral enhancement n-channel (IC gate) MOSFET construction

In a FET, conduction does not occur as it does in the BJT with *minority* carriers. In a BJT, the carriers injected from an emitter migrate across a base,

⁸ An inversion layer can easily be formed by implanting and diffusing a thin n⁺ (or p⁺) layer at the surface under the gate of our npn (or pnp) structure.

and get collected at a collector. In a MOSFET, *majority* carrier conduction occurs when a surface layer gets *inverted* in an enhancement mode device. Inversion by the gate voltage means p material is made to look like n material and vice versa. The inversion layer connects the source and drain. In a depletion mode device the surface is already inverted, can conduct, and can be depleted, that is, shut off by applied gate voltage.

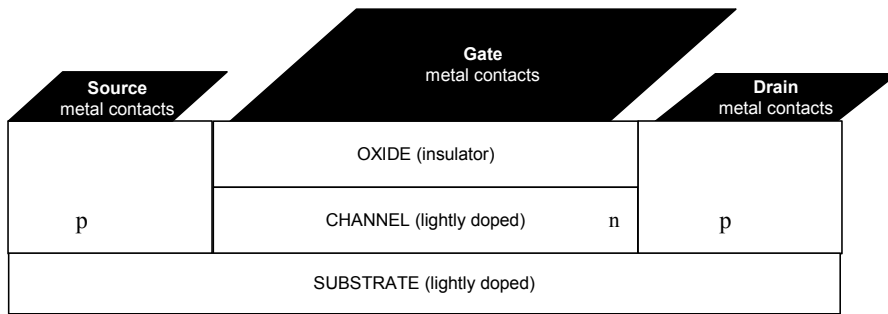


Figure J-9. Typical lateral p-channel (IC gate) MOSFET construction⁹

Today, most ICs are made using enhancement mode MOSFETs. The gate voltage required to bias the transistor into a conducting condition is called the threshold voltage, V_{th} , and conduction occurs when $V_{gs} > V_{th}$ and $V_{ds} > 0V$. The conditions for turning on the various types of MOSFETs are summarized in Table J-1.

Table J-1. Conditions for turning a MOSFET on

MOSFET Type	V_{gs}	Conduction
NMOS Enhancement Mode	$V_{gs} > V_{th}$	Yes
NMOS Depletion Mode	$V_{gs} \leq V_{th}$	Yes
PMOS Enhancement Mode	$V_{gs} < V_{th}$	Yes
PMOS Depletion Mode	$V_{gs} \geq V_{th}$	Yes

The MOSFET has become the dominant form of transistor for discretes and ICs. In no small part, this trend has been driven by both the accessibility of the semiconductor surface and the advances in lithography, enabling ever-smaller transistor geometries to be fabricated.

⁹ To avoid confusion, the contacts are still labeled “metal.” However, today’s deep sub-micron CMOS contacts will probably be implemented in polysilicon.

J.5.5 BJT Versus MOSFET Behavioral Comparison

Parasitic BJT action in a MOSFET and parasitic MOSFET action in a BJT are natural and possible occurrences. Device designers and operators must always be aware that they can be present. They must understand both types of transistors.

Consider whether a BJT surface and oxide can be made clean enough to eliminate all possibilities of inversion. Not in a practical sense. First, all semiconductor surfaces can be made to invert. Second, lattice dislocations (especially at the Si-SiO₂ interface) due to dopant atoms, and hot-electron state injections at the surface and in the oxide, can alter inversion conditions. Throughout the late 20th century, it was relatively easy to invert only moderately high voltage (40 volts BV_{ceo}) pnp BJTs. This meant that few such devices were ever developed without guard or equipotential rings. Guard or equipotential rings are floating rings of highly doped semiconductor material (p⁺ on a p-surface, n⁺ on an n-surface) that are difficult to invert. Such rings surround the base-emitter structures on a BJT topside. One example can be seen in Figure 7-22. The guard rings act like an IC-well does in isolating an active device from its neighbors. In this case, we isolate the active BJT from its die edge. The die edge acts like a near-infinite source of low activation energy current carriers. The ring prevents the surface inversion from reaching the die edge and shorting out the device.

Figure J-10 shows BJT collector characteristic curves that are linearly spaced with I_b , except for low- and high-current non-ideal effects. Figures J-11 and J-12 shows MOSFET curves that are spaced as $(V_{gs}-V_{th})^2$. The BJT curves in Figure J-10 cover a wider voltage range, resulting in an increase in slope as the BJT approaches breakdown. As collector-base reverse-bias junction voltage is increased the junction depletion region widens further — especially on the lightly doped base side. This narrows the region that the minority carriers have to drift across, lessens base recombination and increases beta. Dr. James Early first explained the cause of this behavior in 1952 — thus the name Early effect.

The MOSFET would show a similar upward slope at high voltages if the voltage range were extended. CMOS shows a flatter slope in the normal operating region, and steeper slope above V_{cc} .¹⁰ The sharp increase in current is caused by parasitic diode turn-on in CMOS. In a BJT a large increase in current occurs because of voltage breakdown, but usually at significantly larger voltages than V_{cc} .

¹⁰ CMOS breakdown is caused by two effects: parasitic diode turn on, and gate oxide breakdown. The low-voltage oxide breakdown makes ESD protection very important in submicron CMOS parts.

In a BJT, the Early effect is the name of a base-width-modulation effect due to the reverse-biased V_{bc} magnitude. In a MOSFET, the equivalent effect is called channel-length modulation due to the reverse-biased drain junction (increasing V_{ds} shortens the channel length, and increases current with approximately linear slope).

Both types of devices show approximately linear I-V characteristics below a certain voltage:

- For a BJT, it is $V_{ce} \leq V_{ce(sat)}$.
- For an n-channel MOSFET, it is $V_{ds} \leq V_{gs} - V_{th}$.

We can make some comparisons of BJT and MOSFET operational regions. For example, the saturation region (see Figure J-10) for a BJT corresponds to the ohmic region, also known as the triode region (see Figure J-11 and J-12) in MOSFET. The MOSFET ohmic region is more linear than the BJT saturation region and it covers a much wider voltage range in MOSFET. The saturation region in MOSFET actually corresponds to the linear operation region in a BJT. These regions of operation, linear in BJT and saturation in MOSFET, provide most of the signal gain used in amplifiers and I/O buffers.

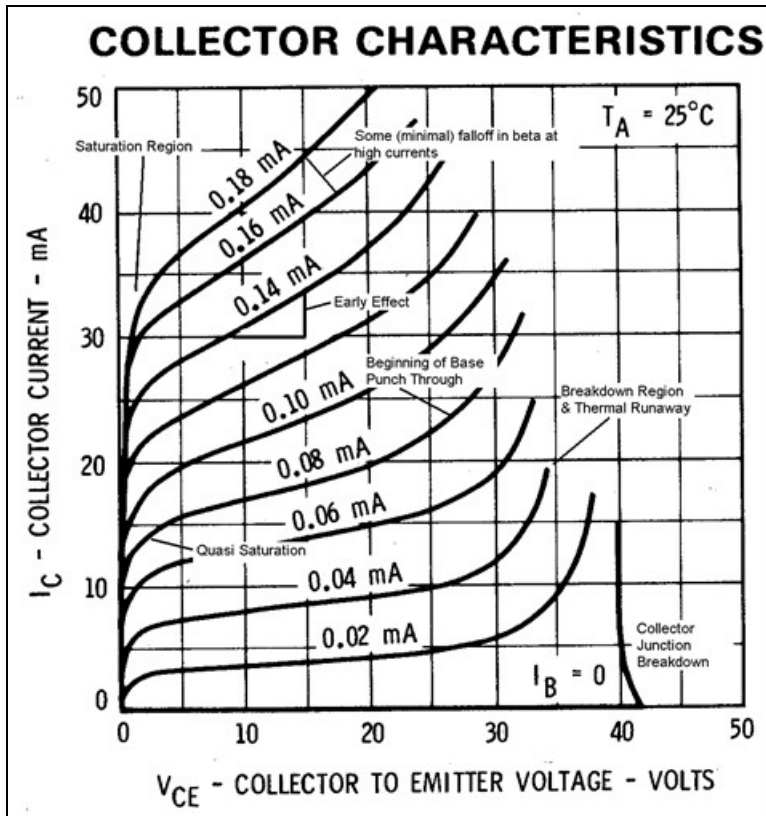


Figure J-10. BJT CE collector characteristic curves, 2N3904 transistor [141]

The key difference between the two types is that a BJT draws DC- I_b , while a MOSFET draws only a tiny gate-leakage¹¹ current (ideally zero). Thus, a BJT consumes significantly more standby power than a MOSFET.

Both BJT and MOSFET can draw relatively large AC currents due to capacitive effects (C_{be} , C_{gs}). Both have an effective feedback capacitance from collector and drain to base and gate (C_{cb} , C_{dg}). A portion of the output signal gets fed back to the input through the feedback capacitance, where the amplifier gain then amplifies the fed back signal. The result makes it appear as though the amplifier gain multiplies the actual capacitance.¹²

¹¹ Plus there is some leakage in the parasitic diodes inherent in the IC structure. This leakage is larger than the gate leakage and is becoming a significant contributor to power consumption in handheld (battery operated) products.

¹² This gain multiplication effect was first explained in vacuum tube amplifiers by J. M. Miller [87] and is called "Miller Effect Capacitance." One also sees a feedforward effect from gate to drain, which is what causes the initial "bump" sometimes seen in CMOS V-T curves.

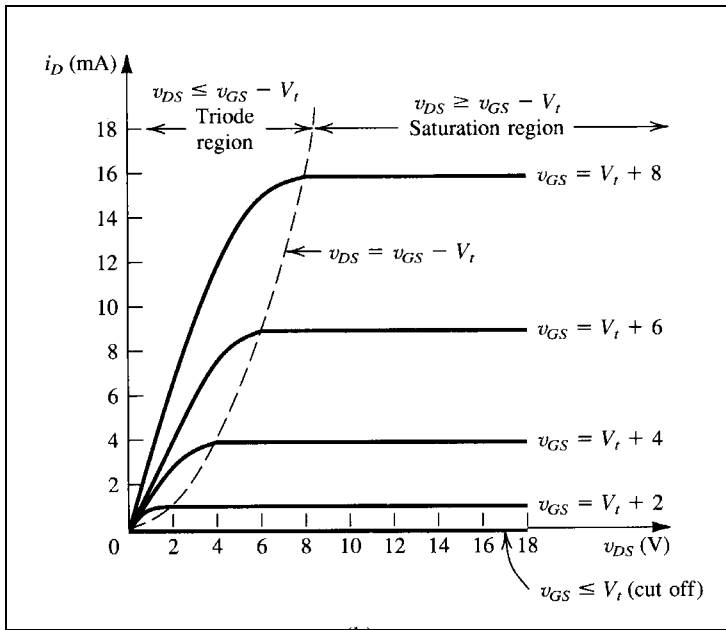


Figure J-11. MOSFET drain characteristic curves, n-channel enhancement mode transistor [108, page 309]

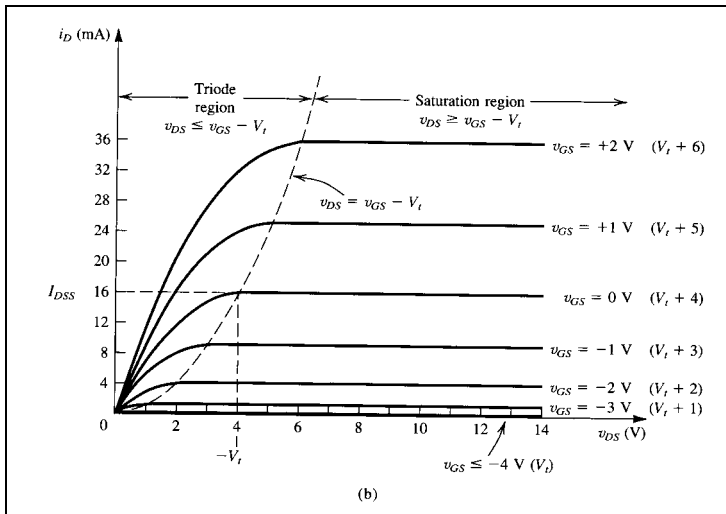


Figure J-12. MOSFET drain characteristic curves, n-channel depletion mode transistor [108, page 320]

Table J-2 summarizes the differences between BJT and MOSFET.

Table J-2. BJT versus MOSFET summary

Property	BJT	MOSFET
Characteristic curves at the output	Evenly spaced with I_b	Evenly spaced as $(V_{gs} - V_{th})^2$
Gain Modulation at the output due to power supply voltage	Base-width changes and Early effect	Channel length changes
Linear output I-V range	For $V_{ce} \leq V_{ce(sat)}$	For $V_{ds} \leq V_{gs} - V_{th}$
Steady-state power consumption	Relatively large because of I_b	Smaller because gate leakage is small

J.6 CALCULATING DEVICE PHYSICS PROPERTIES

J.6.1 Introduction to TCAD and SPICE

TCAD tools are essential to modern semiconductor design and fabrication. For example, TCAD is often used to optimize chip layout using multiple fingers (emitter or drain) to increase speed (by reducing capacitance and series resistance), and to reduce layout area. This activity is usually done for output transistors on both BJT and MOSFET chips, but is a minor activity for logic and input-stage transistors.

The *T* in TCAD stands for Technology, specifically semiconductor process technology. The *CAD* stands for Computer-Aided-Design. TCAD is comprised of a set of algorithms for computing semiconductor behavioral properties based on device physics. This topic presents examples of how device structure (that is, junction depths, channel lengths, doping profile, and geometry) is used in equations derived for computing some TCAD and SPICE parameters. TCAD is the computer aided engineering implementation of the physics models, process models, and SPICE model extraction.¹³ Process models predict such things as implantation depth for dopants and their migration during drive-in diffusion, annealing, and other process steps.

SPICE (Simulation Program with Integrated Circuit Emphasis) is a computer program that was developed to simulate the device physics models as part of a circuit design.¹⁴ Most device models were too complex to readily solve by node and mesh equations. Textbooks on the circuit application of

¹³ Refer to [10, 11, 32, 35, 38, 40, 44, 63, 68, 71, 77, 79, 83, 84, 86, 90, 97, 98, 117, 118, 121, 127, 128, 132, 140].

¹⁴ Refer to [33, 34, 42, 44, 47, 48, 53, 63, 66, 109, 110, 111].

SPICE typically present SPICE parameters as measured properties. Device physics theory is equally as important as measuring the model parameters.

By considering the device-physics equations, we see why SPICE is thought of as a physical model rather than a behavioral model. The device-physics derivations lead to parameters like junction-emission coefficient, and junction-diffusion capacitances, which are related to physical phenomena.

Many SPICE programs are available for device modeling and simulation. Many commercial programs (such as HSPICE®, PSPICE®, Spectre®, Saber®, Aim SPICE®, IntuSoft®, and others) are also available. They are all slightly different from each other. Having no standard SPICE model guarantees that models and simulators will not exchange data seamlessly.

J.6.2 Comparing Different Varieties of SPICE

Different versions of SPICE, SPICE derivatives,¹⁵ and the device physics models on which SPICE is based do not use identical sets of parameters. Default values for parameters can also vary between implementations of models of device types. It is also worth noting that default values are almost always “wrong” for an actual device – for example, parasitic capacitances defaulted to zero, giving a transistor excessively high bandwidth and speed.

J.6.2.1 Capacitor Models

A simple capacitor provides an example of how different versions of SPICE differ. In the original UC Berkeley SPICE, the basic capacitor came in two forms: a fixed capacitor, and a geometric capacitor. The geometric capacitor allowed the user to define the capacitance in terms of physical parameters, such as length, width, sidewall length, and dielectric constant. Neither the fixed nor the geometric capacitor allowed any dependence on voltage or temperature.

In reality, semiconductor capacitance varies with both voltage and temperature. For example, HSPICE allows variation with temperature but not with voltage. IS-SPICE allows variation with temperature or voltage, but not both. Some SPICE simulators, such as HSPICE, IS-SPICE, and PSpice, have added support for user models (equations), making it possible to model capacitor temperature and voltage variations together, as well as modeling non-polynomial variation.

¹⁵ Refer to [10, 35, 40, 63, 68, 69, 79, 83, 84, 86, 100, 103, 118, 132].

J.6.2.2 BJT SPICE Models

BJT SPICE models have more variation between versions of SPICE than does the simple capacitor. Table J-3 compares some selected BJT model parameters.¹⁶

BJT device behavior modeled by these parameters can usually be observed directly on a curve tracer. Phenomena, such as quasi-saturation and high-current beta rolloff, are now incorporated in the models. In addition, the effects of manufacturing and process problems can be seen. Some examples are surface contamination effects on a BJT's low current beta, avalanche breakdown voltages, and surface limited breakdown voltages [74].

Table J-3. Comparison of SPICE parameters with device physics model properties

Parameter	SPICE 3F3 [97]	H-SPICE (1992) [85]	P-SPICE (6/2004) [21]	Ebers- Moll 2 [38]	Gummel -Poon [98]	VBIC (2002) [22]
Model selector		LEVEL				AJE, AJC, AJS
Substrate connector selector		SUBS				
Saturation current	IS	IS	IS	IS	I_S	IS
Reverse BC saturation current		IBC				
Reverse BE saturation current		IBE				
Substrate p-n saturation current		ISS	ISS			
Ideal max forward bias Beta	BF	BF (BFM)	BF	BF	β_F	IBEI
Forward current emission coefficient	NF	NF	NF	NF	N_F	NEI+ TNF
Forward Early voltage	VAF	VAF+TVAF1, TVAF2 (VA, VBF)	VAF (VA)	VA	V_{AF}	VEF
Corner for BF high current rolloff	IKF	IKF+TIKF1, TIKF2 (IK, JBF)	IKF (IK)		I_{KF}	IKF
High current rolloff coefficient		NKF	NK			
B-E leakage saturation current	ISE	ISE+TISE1, TISE2	ISE (C4, JLE)			IBEN
B-E leakage emission coefficient	NE	NE+TNE1, TNE2 (NLE)	NE			NEN

¹⁶ Refer to Table J-6 for MOSFET model parameters.

Parameter	SPICE 3F3 [97]	H-SPICE (1992) [85]	P-SPICE (6/2004) [21]	Ebers- Moll 2 [38]	Gummel -Poon [98]	VBIC (2002) [22]
Reverse current Beta	BR	BR+TBR1, TBR2 (BRM)	BR	BR	β_R	IBCI
Reverse current emission coefficient	NR	NR+TNR1, TNR2	NR	NR	n_R	NR/ NCI
Reverse Early voltage	VAR	VAR+TVAR1, TVAR2 (VB, VRB, BV)	VAR (VB)		V_{AR}	VER
Corner for reverse beta rolloff	IKR	IKR+TIKR1, TIKR2 (JBR)	IKR		I_{KR}	IKR
B-C leakage saturation current	ISC	ISC+TISC1 , TISC2 (C4, JLC)	ISC (C4)			IBCN
B-C emission coefficient	NC	NC+TNC1, TNC2 (NLC)	NC			NCN
Zero bias base resistance	RB	RB+TRB1, TRB2	RB+TRB1, TRB2	RB	r_B	RBI, RBP
Current where RB falls to 1/2 min	IRB	IRB+TIRB1, TIRB2 (JRB, IOB)	IRB			
Min RB at high current	RBM	RBM+TRBM1, TRBM2	RBM+TRM1, TRM2			RBX+ XRB
Emitter resistance	RE	RE+TRE1, TRE2	RE+TRE1 , TRE2	RE	r_E	RE+ XRE
Collector resistance	RC	RC+TRC1, TRC2	RC+TRC1, TRC2	RC	r_C	RCX+ XRC
B-E zero bias depletion capacitance	CJE	CJE	CJE	CJE	C_{be0}	CJE
Distributes CJE between inner & outer base						WBE
B-E built-in potential	VJE	VJE+TVJE (PE)	VJE (PE)	PE	ϕ_{be}	PE
B-E junction exponential factor	MJE	MJE+TMJE1, TMJE2 (ME)	MJE (ME)	ME	m_{be}	ME
Ideal forward transit time	TF	TF+TTF1, TTF2	TF	TF	τ_F	TF & QTF
Coefficient for base dependence of TF	XTF	XTF	XTF			XTF

Parameter	SPICE 3F3 [97]	H-SPICE (1992) [85]	P-SPICE (6/2004) [21]	Ebers- Moll 2 [38]	Gummel -Poon [98]	VBIC (2002) [22]
Voltage describing VBC dependence of TF	VTF	VTF	VTF			VTF
High current parameter for TF	ITF	ITF+TITF1 , TITF2 (JTF)	ITF			ITF
Excess phase @ frequency $1/(2\pi TF)$ Hz	PTF	PTF	PTF			TD
B-C zero bias depletion capacitance	CJC	CJC	CJC	CJC	C_{bc0}	CJC, CJEP, XCJC
B-C built-in potential	VJC	VJC+TVJC (PC)	VJC (PC)	PC	ϕ_{bc}	PC
B-C exponential factor	MJC	MJC+TMJ C1, TMJC2 (MC)	MJC (MC)	MC	m_{bc}	MC
Fraction of CJC connected to internal base node	XCJC	XCJC (CDIS)	XCJC			
Fraction of CJC connected internally to Rb			XCJC2			
Ideal reverse transit time	TR	TR+TTR1, TTR2	TR	TR	τ_R	TR
Zero bias collector substrate capacitance	CJS	CJS (CCS, CSUB)	CJS (CCS)		C_{CS0}	CJCP
Fraction of CJS connected internally to Rc			XCJS			
Substrate junction built-in potential	VJS	VJS+TVJS (PSUB)	VJS (PS)		ϕ_{cs}	PS
Substrate p-n emission coefficient		NS	NS			
Substrate junction exponential factor	MJS	MJS+TMJ S1, TMJS2 (ESUB)	MJS (MS)	MS	m_{cs}	MS
Forward and reverse Beta temperature	XTB	XTB				XII & XIN

Parameter	SPICE 3F3 [97]	H-SPICE (1992) [85]	P-SPICE (6/2004) [21]	Ebers- Moll 2 [38]	Gummel -Poon [98]	VBIC (2002) [22]
coefficient						
Energy gap for temperature effect on IS	EG	EG+GAP1, GAP2	EG	EG	eg	EA ¹⁷
Temperature coefficient for effect on IS	XTI	XTI	XTI (PT)			XIS
Flicker noise coefficient	KF	KF	KF			
Flicker noise exponent	AF	AF	AF			
Coefficient for forward bias depletion coefficient	FC	FC	FC			FC
Quasi-sat model flag for temperature dependence			QUASIM OD			
Quasi-sat temp. coefficient for hole mobility			CN			
Quasi-sat temp. coeff. for scattering limited hole carrier velocity			D			
Quasi-saturation extrapolated bandgap voltage @ 0°K			VG			
Epi region charge factor		QCO	QCO			QCO
Epi region resistance		RCO	RCO			RS+ XRS
Quasi-sat coefficients?						CI, HRCF
Carrier mobility knee (velocity saturation) voltage		VO	VO			VO+ XVO
Epi region doping factor		GAMMA	GAMMA			GAM M
Reverse beta for substrate BJT		BRS				
Emission coefficient		NEPI				
External constant		CBCP				CBC0

¹⁷ There is a series of model/temperature dependent energy gaps: EAIE, EAIC, EAIS, EANE, EANC, EANS & TAVC

Parameter	SPICE 3F3 [97]	H-SPICE (1992) [85]	P-SPICE (6/2004) [21]	Ebers- Moll 2 [38]	Gummel -Poon [98]	VBIC (2002) [22]
capacitor, base- collector						
External constant capacitor, base- emitter		CBEP				CBE0
External constant capacitor, collector- substrate		CCSP				
Temperature derating factors		CTC, CTE, CTS				
Absolute temperature			T_ABS			
Measured temperature	TNOM		T_MEAS URED			TNO M & TAM B
Relative to current temperature			T_REL_ GLOBAL			
Relative to AKO model temperature			T_REL_ LOCAL			
Self heating effects						RTH, CTH
Avalanche effects						AVC1 , AVC2
Parasitic transistor parameters ¹⁸						
Area scaling factors	Various	Various	Various	Various	Various	Variou s

High current beta rolloff coefficient is a particularly important example of the issue that not all models have the same parameters. If a SPICE simulator reports “unused parameter,” this indicates that there is a mismatch between a parameter set and the model the SPICE simulator is using the parameters in. The user must then either find the correct parameters for the model, or the correct model for the parameter set.

BJT device behavior model by the above parameters can, for the most part, be observed directly on a curve tracer. Phenomena such as quasi-saturation, high current beta rolloff, and more are now incorporated in the models. In addition, the effects of manufacturing and process problems can

¹⁸ There is a model of parasitic transistors with parameters: ISP, NFP, WSP, BEIP, IBENP, IBCIP, NCIP, IBCNP, NCNP & IKP.

be seen. For example, surface contamination effects on a BJT's low current beta. Also avalanche, and surface limited breakdown voltages, and much more. One of us, [Leventhal, 59] has written an unpublished monograph, *Device Physics Diagnostics by Curve Tracer*, on this subject.

J.6.3 How Structural Design Influences BJT Performance

From the original point-contact BJT transistor¹⁹ to modern deep sub-micron ICs, semiconductor process technologies have undergone many developments, evolutions, and revolutions.

The original semiconductor crystals pulled from a crucible of molten material (most likely germanium) averaged barely ½ inch in diameter and a few inches long. Today's crystals are larger than 12 inches in diameter and a few feet long. For many years, silicon has reigned as king of semiconductor materials despite the superb properties of other materials like Gallium Arsenide. Once the semiconductor crystal is grown, it is sliced like a loaf of bread into many thin wafers known as substrate wafers.

The substrate wafers, usually heavily doped and with a high conductivity, become a matrix upon which a gas deposits an epitaxial (epitaxial means “grown upon”) layer. From this point, we could construct technologies like Mesa Transistors, which are still used in high power discrete transistors. But the dominant technology is the Silicon Planar Process [53]. Semiconductor devices are created in the epitaxial layer. For integrated circuits composed of multiple individual transistors, one or two layers of polysilicon, separated by oxide, are used to form “local” interconnects. Alternate layers of insulator and metal are grown above the poly layers. Eight or more layers of copper may be used for “global” interconnects. The resistance of polysilicon is too high to use for global interconnects.

Some device design structural-dopant concentration choices for optimizing different electrical performances are shown in Table J-4. These optimizations show up in the electrical performance characteristic curves of devices. These characteristic curves can be used to compare and contrast component performance.

¹⁹ Point-contact transistors came first. They have the metal wires touching the p or n material, almost creating Schottky junctions. The junction transistor came next, where they put dots of indium or gallium onto the germanium, then melted/diffused it into the germanium at high temperature. Thus an n-emitter (p) and n-collector (p) were diffused into a block of p (n) material. Diffused transistors, where a gas containing the dopant compound would break down at high temperatures, and then diffuse into the wafer, were third-generation transistors.

Table J-4. Small-signal BJT semiconductor device construction

Type	Description
Low Level - Low current - Low Noise	Typically 10x15 mils die with low overall doping. Features rapid low-current β turn-on, high input impedance and low 1/f audio noise. Superseded by JFET technology. High breakdown voltages (BV _{ceo} of 40V, I _c of 50mA). But poor power-handling capacity.
General Purpose	Typically from 10x15 to 250x250 mils die. All-around devices intended to fit most applications moderately well. Drive currents from about 200mA to 50A and BV _{ceo} breakdowns from 30V to 200V. Gain bandwidths of about 300MHz at the low-power end to 1MHz at the high-power end.
RF Amplifiers, Oscillators and Mixers	Typically not much larger than 10x15 mils to minimize capacitances. Many construction innovations to optimize gain bandwidths of 900MHz and beyond: Ballasted emitters, steeply graded junctions, graded base, Faraday shields, high emitter periphery to area, and high overall doping to minimize high-current β roll-off. Breakdowns usually below 15V and drives from a few tens to perhaps 200mA at best. A whole variety of RF types (as diverse as most of the categories discussed here put together) were developed by Motorola. But that discussion is too much for the purposes of gaining insight into semiconductor modeling.
Saturated Logic Switches	Typically 10x15 mils to perhaps 22 mils square. Somewhat similar to RF types (for high edge rate). Sometimes gold- (npn) or platinum- (pnp) doped to kill base minority-carrier storage time. Rise/fall times down to 1-2ns and turn-on/turnoff of 15ns on the smaller devices. Breakdown voltages 10-to-15-volts. Higher leakage currents because of the gold/platinum enhanced recombination centers.
High Voltage Video Amplifier - Driver	One example is a 30 mils square die. Optimized for high breakdown voltage and rugged 2nd Breakdown Safe Operating Area capability with several construction features. Including: extra-thick base and collector regions, junction field plate, deep diffusions, triple (collector) diffused, surface-isolation guard / equipotential rings and extra-clean processing. Gain-bandwidth of 80MHz, I _c max of 250mA and 300V BV _{ceo} breakdown. Used for CRT video circuit drive.
Switchmode Power Switches	Larger die - 200 mils square and larger. Higher overall doping levels. Low saturation voltages. Characterized and optimized for fast switching speed at high voltages and currents. Rugged Safe Operating Area capability. Breakdown voltages to 800V and switching currents to 20A - not in the same device.
Darlington Amplifiers and Switches	Achieves β multiplication with two transistors on one die in emitter follower cascade. About 30 mils square die with the same general characteristics as general-purpose types. From here to the concept of integrated circuit is not a great distance. Cascaded β s of 1000 to 15,000 depending on the device.

J.6.4 Modern Semiconductor Process Control

Today, TCAD software is used extensively to design devices, generate their SPICE (typically HSPICE, Spectre, or Eldo) model parameters, and control the processes used in their manufacture. A SPICE model library is normally not portable between simulator platforms.²⁰ When requesting models from a foundry, it is important to specify the simulator, as well as the process name. Foundries typically offer BSIM and the Enz-Krummenacher-Vittoz (EKV) models for these three simulators. As a result, HSPICE is losing its once dominant lead in these applications.

Most semiconductor manufacturers use these TCAD programs to control their processes—not to generate simulation models. Consequently, the SPICE models produced may be less desirable for circuit simulation purposes.

For example, Figure J-13 shows two sets of I-V data for a diode used in an I/O buffer design. On the left, the SPICE and IBIS models match almost exactly. On the right, the SPICE and test data do not match. The mismatch could have been caused by an incorrect model parameter, or by an underlying model problem internal to SPICE. The causes of this mismatch are related to different understandings of the correct voltage range over which to measure clamp behavior.

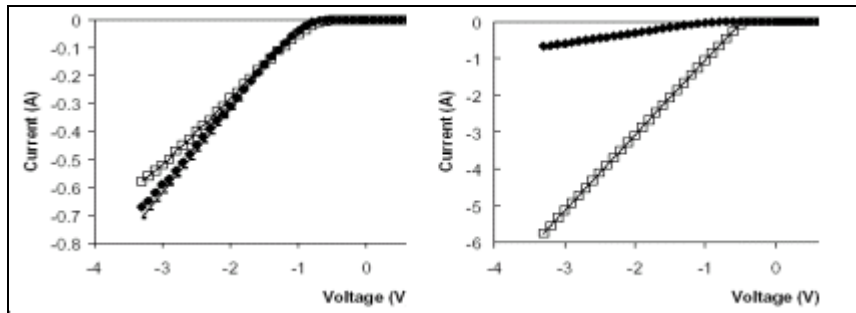


Figure J-13. SPICE and IBIS models compared to measured data for a clamp diode: data courtesy of Cypress Semiconductor

J.6.5 More About SPICE and TCAD

In the context of SPICE, the term netlist refers to the list of components and connections for a circuit. Also in the context of SPICE, the term model refers to one or more of the following:

²⁰ A model parameter for a different simulator might not cause a particular simulator to “crash”, it can, and will, generate incorrect currents and voltages.

- A schematic of a circuit
- A netlist
- A subcircuit or macromodel
- A parameter set for a particular transistor
- A library of model parameters for a specific technology
- The simulator's equations, coded to use these parameters

Equations are coded differently in different SPICE models—or even the same model in different SPICE programs. For example, HSPICE has over 50 different MOSFET models, each with its own set of parameters. The parameters can be significantly different from one model to the next. For example, the equations for the same transistor model can have:

- Different names for the same parameter
- Different values for the same parameter name
- Different parameters (no name match)

TCAD addresses all aspects of semiconductor design, including such issues as die interconnections. TCAD at the IC chip level sometimes also addresses Signal Integrity, current density, electromigration on the interconnections, EMI, package design, and many other concerns. Some SPICE parameters, like beta and Early effect, are also familiar to SPICE model circuit designers. But there are other device physics TCAD properties that are not used in SPICE. An example is breakdown voltage.²¹ This is because SPICE, a program for circuit analysis, uses only a subset of the formulas and properties available to device designers. Also, many SPICE models (parameter sets) do not model reverse-bias operation or second-order effects accurately.

Designing a semiconductor is more than designing its desired behavior as an amplifier or a switch, as addressed in SPICE. For instance, what about its current, voltage, and power handling capabilities? What about electromigration and reliability issues? These issues can be modeled with a combination of equations from device physics and parameters from measurements.

²¹ Equations for computing collector saturation voltage and breakdown voltage for BJTs are presented in “Appendix J, Device Physics.”

J.7 EXAMPLES OF COMPUTING ELECTRICAL PROPERTIES FROM STRUCTURE

For most IC processes, the fabricator and foundry take care of computing and extracting transistor parameters. This topic of parameter computation and extraction is included to show:

- The connection with modeling
- That there are ways to verify the reasonableness of parameters²²
- How formulas are used to compute SPICE and TCAD values

J.7.1 Selected Semiconductor Constants and Quantities

Before we discuss the device physics equations, let us examine some of the parameters understood as defined constants and quantities. Some SPICE models calculate parameters from other quantities, and it helps to understand how that is done. Many of the defined constants and quantities can be computed from more fundamental physical properties and semiconductor technology processes. For example, N_{DB} (base doping density) is one such quantity.

Once parameters are defined, they should not have to be re-defined. Table J-5 lists these defined constants and quantities.

Table J-5. Parameters in the structure-based equations (J-1) to (J-8) and (J-18) to (J-22)

Parameter	Description
D_{nE}	Electron diffusion coefficient
D_{pB}	Hole diffusion coefficient
N_{DB}	Base doping density
N_{AE}	Emitter doping density
W_E	Width of the emitter region
W_B	Neutral (active) base width
W_{EB}	Width of the emitter-base region
L_{pB}	Diffusion length of minority carriers in the base
τ_p	Lifetime of holes
τ_o	Excess minority carrier lifetime
V_{EB}	Emitter-Base junction bias voltage
n_i	Equilibrium intrinsic carrier (holes or electrons) concentrations
q	Charge magnitude on the electron = 1.60×10^{-19} coulomb
$K_b = k_b$	Boltzman's constant: 1.38×10^{-23} Joules/Kelvin
T	Temperature in degrees Kelvin

²² The Fabless Semiconductor Association (<http://www.fsa.org/>) has set up a model quality committee on verifying parameters.

Parameter	Description
E _g	Energy band gap of the silicon material
ε ₀	Permittivity of free space = 8.86*10 ⁻¹⁹ F/cm
ε _R	Relative permittivity of silicon = 11.7
μ _n	Mobility of electrons. Mobility depends on the intrinsic semiconductor material (silicon, germanium, GaAs, etc.) and the doping concentration that has been added to it.
μ _p	Mobility of holes. Mobility depends on the intrinsic semiconductor material (silicon, germanium, GaAs, etc.) and the doping concentration that has been added to it.

Our discussion about device physics thus far represents a simplified theory without taking into account such things as emitter de-biasing, Early effect, high current injection effects, surface recombination and so on. For the most part, these additional effects are accounted for by other terms in the Gummel-Poon/Ebers-Moll/hybrid-pi (that is, SPICE) model.

For an npn, the base is doped with acceptors (p) and emitter with donors (n). The (n) and (p) subscripts should be swapped for a pnp. Investigating a little deeper into how BJT parameters can be calculated:

$$D_{nE} = \left(\frac{k_b T}{q}\right) \mu_n \quad (\text{J-1})$$

Equation (J-1) is also known as Einstein's relationship.

$$D_{pB} = \left(\frac{k_b T}{q}\right) \mu_p \quad (\text{J-2})$$

Parameters N_{DB} and N_{AE} are found from the physics and chemistry of the doping, ion implant, and diffusion process. That set of processes has its own set of formulas, charts, and constants. Calculating those quantities is usually in the realm of the material scientists and process engineers. Calculating a device's doping profile as a result of its processing is the usual way of finding NDB, NAE, WE, and WB. These parameters are static once set by the starting material, epi growth, oxide growth, doping, diffusion, masking, and other processing of the device.

The emitter-base space-charge region has some dynamic characteristics because its width changes with applied bias. As it changes, the effective widths of the depletion layer and base width also change. This is because depletion regions grow and shrink on either side of a junction due to the applied bias. The change mostly occurs on the lightly-doped base side.

Consider the static equilibrium case with no applied bias.

Then:

W_0 is the width when $V_{eb} = 0V$

$$W_0 = \sqrt[3]{12 \epsilon_s \epsilon_0 \phi_B / qa} \quad (J-3)$$

Where:

a = the dopant concentration gradient at the junction²³

ϕ_B = the built-in junction potential = $\phi_{Fp} + |\phi_{Fn}|$, or the sums of the Fermi potentials.

ϕ_B becomes $\phi_B \pm |V_j|$ in equation (J-3) when bias is applied. Reverse bias widens the space-charge region, forward bias narrows it. V_j is, of course, V_{EB} in this discussion.

Next:

$$L_{pB} = \sqrt{D_p \tau_p} \quad (J-4)$$

Where:

D_p is the diffusion constant of holes.²⁴ The quantity n_i is found from Fermi level statistics and, at thermal equilibrium, we have:

$$n_i^2 = N_c N_v e^{-E_g / k_b T} \quad (J-5)$$

Where:

N_c is the number of states at the conduction band

N_v is the number of states at the valence band

and:

$$n_i^2 = np \quad (J-6)$$

Where:

²³ This is why the SPICE equations fail for many modern devices. The junction can be graded in a “non-exponential, non-linear” fashion, where the peak in doping is not at the junction, but deeper in another part of the region.

²⁴ More information on diffusion, recombination lifetimes, hole/electron mobilities, and etc., can be found in [47, pages 101-112].

n is the number of electrons (carriers) primarily due to doping
 p is the number of holes (acceptors) primarily due to doping

Note that $np = \text{constant}$. Doping with Nd increases n and reduces p, and doping with Na increases p and reduces n. In all equations, one could specify $n(E)$ vs. $n(B)$ and $p(E)$ vs., $p(B)$. For example, equation (J-6) is equivalent to:

$$n(E) * p(E) = ni^2 \quad (J-7)$$

$$n(B) * p(B) = ni^2 \quad (J-8)$$

J.7.2 Methods for Refining Models

There are two common modeling approaches to account for “extensions” to a basic model. The quick (and easy) solution is to change equations and add more parameters until a model fits measured data better. This is the approach used in the series of BSIM MOS models. The other approach is to understand the physics and then modify the equations and add selected parameters as needed. This is the approach is used for the EKV MOS model. The second approach leads to more accurate models that are easier to update as new physical effects become significant.

J.8 EXAMPLES OF SPICE MODELS AND PARAMETERS

SPICE parameters are used in the diode and MOSFET (CMOS) equations to compute the circuit behavior of those devices. However, the BJT equations show how the BJT SPICE parameters are derived from semiconductor device structure and materials.

J.8.1 The Diode

Semiconductor diodes predate the invention of any form of transistor. The structure of nearly any type of semiconductor inherently includes one or more diodes, intentional or not (parasitic). FET leakage junctions are basically parasitic diodes and their leakage has come to dominate over gate leakage. Clamp diodes are more often designed into digital I/Os, for limiting reflection overshoot and to provide ESD protection, than not.

J.8.1.1 Diode Equivalent Circuit

A diode is a single p-n junction. Under forward bias, electrons move from the n to the p region and holes move from the p to the n region. Under reverse bias, a leakage current flows between the two regions. Most of the reverse current usually results from increased carrier generation and reduced carrier recombination in the widened depletion region, rather than from electrons and holes moving across the depletion region.

A diode has the same breakdown mechanisms as for the collector-base junction described above, including avalanche breakdown, corner and surface breakdown, and reach-through or punch-through-limited breakdown. Diodes, when both sides are highly doped, can also suffer from Zener breakdown, where electrons quantum-mechanically tunnel through the junction, resulting in low breakdown voltages. Interestingly, many so-called Zener diodes are actually low-voltage-breakdown avalanche diodes.

Figure J-14 shows the circuit symbol for a diode. The p side is labeled NA (the anode) and the n side is labeled NC (the cathode).

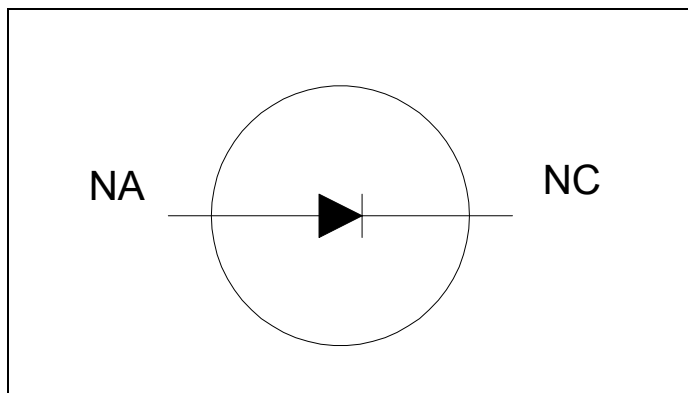


Figure J-14. Diode schematic symbol [84]

Figure J-15 shows a physical cross-section built as a lateral structure, as would be the case where a diode was part of an IC chip, and as opposed to a vertical structure as in the case of discrete diodes.

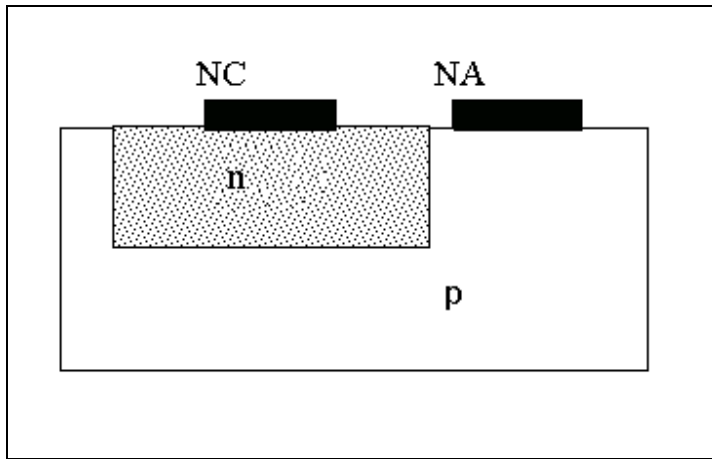


Figure J-15. Diode cross-section

J.8.1.2 SPICE Diode Parameters

As with the bipolar transistor, the SPICE equations and associated parameters are based on the device physics. The default SPICE parameters are for an ideal small-signal diode having infinite bandwidth.

Unlike the transistor, the diode junction is more likely to have high-injection effects at high forward bias. The junction current depends on three effects: the series resistance due to the bulk silicon, the ideal current that varies as $\exp(V/V_t)$, and a second-order effect that varies as $\exp(V/2V_t)$. The SPICE diode model has two parameters: R_S for the resistance and N for the average of the first and second-order current terms. Diode switching times are determined by two factors:

- Junction capacitance, which is determined by the diode's junction voltage.
- Transit time, which is the time required for a hole or electron to cross the undepleted region.

This second effect is accounted for in the SPICE model by the parameter TT . It can be measured using an oscilloscope. TT corresponds to the time from when the bias voltage is changed to when the current starts to change. This time can be relatively long for high-voltage-breakdown diodes, and is faster for integrated-circuit diodes. The default values for $CJ0$ and TT are 0.0

in SPICE, which represents an infinite bandwidth. Table J-6 lists the SPICE diode parameters for equations (J-9) to (J-17).

Table J-6. SPICE diode model parameters [84]

Name	Parameter	Units	Default Value	Effect of Area
IS	Saturation current	A	1e-14	*
RS	Ohmic resistance	Ohms	0	/
N	Emission coefficient		1	
TT	Transit time	sec	0	
CJO	Zero bias junction capacitance	F	0	*
VJ	Junction potential	V	1	
M	Grading coefficient		.5	
EG	Activation energy	eV	1.11	
XTI	Saturation current temperature coefficient		3	
KF	Flicker noise coefficient		0	
AF	Flicker noise exponent		1	
FC	Coefficient for forward bias depletion capacitance		.5	
BV	Reverse breakdown voltage		Infinity	
IBV	Current at breakdown voltage		1e-3	

J.8.1.3 Diode SPICE Equations

Forward Voltage:

$$VT = K_b * (T / q) \quad (J-9)$$

= thermal voltage = .025875 electron
volts @ room temperature (27°C).

Diode Current:

$$ID = IS * (e^{(VD / (N * VT))} - 1) \quad (J-10)$$

In SPICE, the above equation applies in both forward and reverse operation, although it neglects generation and recombination effects that are actually dominant in reverse bias.

Reverse Breakdown Current:

$$IR = IBV * (e^{-(VD+BV)/VT}) \quad (J-11)$$

Reverse-Bias Junction Capacitance:

$$CD = CJO / (1 - (VD / VJ))^M \quad (J-12)$$

Forward-Bias Junction Capacitance:

$$CD = (CJO / (1 - FC)^{(1+M)}) * \{1 - FC(1 + M) + M(VD / VJ)\} \quad (J-13)$$

Charge Storage (due to minority-carrier injection):

$$QS = TT * IS * (e^{(VD/(N*VT))} - 1) \quad (J-14)$$

Where:

$$TT = TS / \ln(1 + IF / IR) \quad (J-15)$$

Where:

IF = the forward current

IR = the reverse current

TS = the storage time

This is not a definition of TT, but a way to calculate TT from measurement of TS, IF, and IR. TT is a SPICE parameter. The value of TS depends on the circuit, so it is not a device parameter. And:

Many versions of SPICE can also calculate signal noise. For example, Shot and Flicker Noise:²⁵

$$in^2 / df = 2 * q * ID * (KF / f) * (ID)^{AF} \quad (J-16)$$

²⁵ Noise (as used in this equation) is the random and spontaneous fluctuations in the current or voltage signals in the semiconductor device. This type of noise is usually of little consequence in digital switching circuits but is important in analog amplifier circuits. Measured noise is usually classified into thermal, flicker (1/f), or shot noise.

Where:

i_n is the spectral noise current

f is the frequency

df is the frequency interval

Effect of Temperature on Parameters:

$$IS@T = IS_{NOM} * (T / T_{NOM})^{(XTI / N)} * e^{(EG / (N * VT)) * (T - T_{NOM}) / T_{NOM}} \quad (J-17)$$

It is interesting to note which physical effects are not modeled in the above diode model. Consequently, they have no parameters. In particular, current to the edges and corners (perimeter) of the diode structure are not modeled in this model. The effect of changing depletion width on RS and TT are not modeled. Hyperabrupt junctions ($M > 1$) are not allowed. Increase in leakage due to recombination-generation effects are modeled only through BV and IBV parameters. Self-heating effects are not modeled. The model user must decide which of these effects need to be modeled, and create a macromodel (subcircuit) to add them.

J.8.2 The Bipolar Junction Transistor (BJT)

J.8.2.1 BJT Equivalent Circuit

The bipolar transistor model in SPICE is based on the Gummel-Poon equivalent circuit, shown in Figure J-16. All of the capacitors and current sources are bias-dependent, as is RB. RC and RE are constant resistance. Also, the default values of the capacitors and base transit time are 0.0, which represents an infinite bandwidth.

The SPICE model accounts for base transit time based on base width but does not fully model base charge storage.²⁶ The model does not account for any collector transit time. This mainly affects accuracy for high-voltage switching BJTs. The model assumes that the emitter-base and collector-base junctions do not go into breakdown. These additional physical effects can be addressed by embedding a BJT inside a larger subcircuit that models these effects.

²⁶ This model does not include base storage–transit time effect correctly. Some people actually use the GaAs bipolar model instead, using silicon parameters, of course.

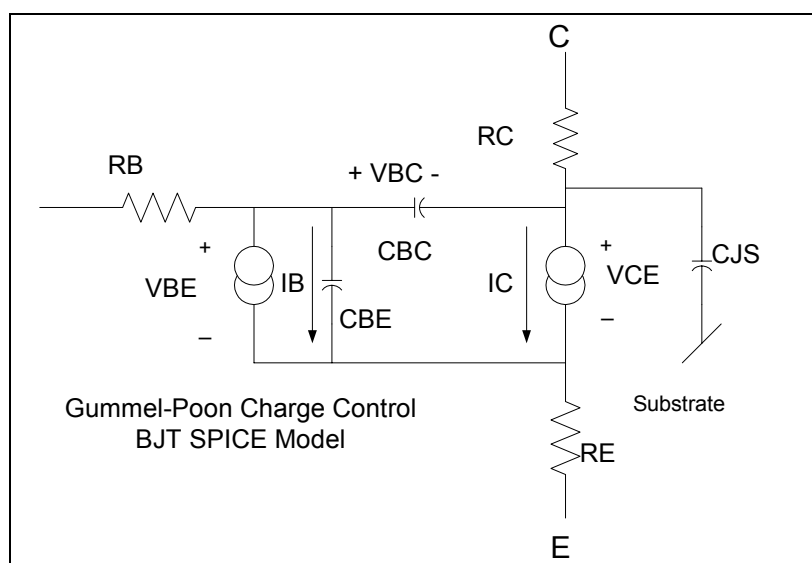


Figure J-16. BJT Gummel-Poon equivalent circuit [84]

J.8.2.2 SPICE BJT Parameters

As with the diode, the SPICE bipolar transistor equations and associated parameters are based on the device physics. The default SPICE parameters are for an ideal small-signal BJT having infinite bandwidth. Table J-7 is a list of the SPICE BJT parameters.

Table J-7. SPICE - Gummel-Poon BJT model parameters [84]

Name	Parameter	Units	Default Value	Effect of Area
IS	Saturation current	A	1e-16	*
BF	Ideal max forward bias Beta		100	
NF	Forward current emission coefficient		1	
VA	Forward Early voltage	V	Infinity	
IKF	Corner for BF high current rolloff	A	Infinity	*
ISE	B-E leakage saturation current	A	0	*
NE	B-E leakage emission coefficient		1.5	
BR	Reverse current Beta		1	
NR	Reverse current emission coefficient		1	
VAR	Reverse Early voltage	V	Infinity	
IKR	Corner for reverse beta rolloff	A	Infinity	*
ISC	B-C leakage saturation current	A	0	*
NC	B-C emission coefficient		2	

Name	Parameter	Units	Default Value	Effect of Area
RB	Zero bias base resistance	Ohms	0	/
IRB	Current where RB falls to 1/2 min	A	Infinity	*
RBM	Min RB at high current	Ohms	RB	/
RE	Emitter resistance	Ohms	0	/
RC	Collector resistance	Ohms	0	/
CJE	B-E zero bias depletion capacitance	F	0	*
VJE	B-E built-in potential	V	.75	
MJE	B-E junction exponential factor		.33	
TF	Ideal forward transit time	sec	0	
XTF	Coefficient for base dependence of TF		0	
VTF	Voltage describing VBC dependence of TF	V	Infinity	
ITF	High current parameter for TF	A	0	*
PTF	Excess phase @ frequency $1/(2\pi TF)$ Hz	degrees	0	
CJC	B-C zero bias depletion capacitance	F	0	*
VJC	B-C built-in potential	V	.75	
MJC	B-C exponential factor		.33	
XCJC	Fraction of CJC connected to internal base node		1	
TR	Ideal reverse transit time	sec	0	
CJS	Zero bias collector substrate capacitance	F	0	*
VJS	Substrate junction built-in potential	V	.75	
MJS	Substrate junction exponential factor		0	
XTB	Forward and reverse Beta temperature coefficient		0	
EG	Energy gap for temperature effect on IS	eV	1.11	
XTI	Temperature coefficient for effect on IS		3	
KF	Flicker noise coefficient		0	
AF	Flicker noise exponent		1	
FC	Coefficient for forward bias depletion coefficient		.5	

J.8.2.3 BJT Physics Equations

Computing β of a BJT

Beta is a SPICE model parameter. Consider the DC current gain (β) of a Bipolar Junction Transistor (BJT) from [47, page. 220]:

$$\beta = h_{FE} = \frac{\gamma\alpha_T}{1 - \gamma\alpha_T} \quad (\text{J-18})$$

In a modern BJT, we want $\gamma\alpha_T$ (γ = emitter efficiency, α_T = base transport factor) to be as close to 1 as possible. This gives a transistor with a large forward β . We can then write:

$$1/\beta \cong 1 - \gamma\alpha_T \quad (\text{J-19})$$

The next step is to formulate a structure and material properties-based equation.

$$\frac{1}{\beta} \approx \underbrace{\frac{N_{DB}W_B}{D_{pB}} * \frac{W_{EB}/\tau_o}{2n_i e^{qV_{EB}/2k_bT}}}_{(a)} + \underbrace{\frac{N_{DB}W_B}{D_{pB}} * \frac{D_{nE}}{N_{AE}W_E}}_{(b)} + \underbrace{\frac{1}{2} * (W_B / L_{pB})^2}_{(c)} \quad (\text{J-20})$$

The first term (a) is a current carrier loss due to the recombination of injecting carriers (from the emitter) within the emitter-base space charge/depletion/junction region. As W_B decreases due to Early Effect, Beta increases. It also decreases the physical region for recombination in the second term.

The second term (b) is a current carrier loss due to the reverse injection and recombination into the emitter from the base, of carriers of the opposite polarity to the emitter-carrier polarity.

These two terms together make up the emitter injection efficiency, γ .

The third term (c) is a current carrier loss due to the recombination of minority carriers within the neutral base. It is also known as the base transport factor, α_T .

In summary, as the loss factors decrease, the beta of the BJT increases. Early SPICE models did not model the recombination-generation current change with base width, and did not model low- versus high-level injection effects.

The Beta we have just computed from structure in equation (J-20) is the BF in Table J-7.

Beta Refinements and Non-Ideal Effects

At very low currents, the carrier recombination loss predominates over other losses in the base. The losses of majority carriers injected from the base occur during diffusion into the emitter-base space-charge region and then into the emitter. These losses are fixed. As current increases, they become insignificant. Carrier-recombination losses in the neutral base are a fixed percentage of total current. As current increases, the neutral base current losses become predominant. This gives rise to the classical low-current beta rolloff and rollup of a BJT. This behavior is difficult to see on a scan of collector characteristic curves on a curve tracer—as opposed to a plot of beta versus I_c . Figure J-17 shows an unusual example of high current carrier losses in the low-current region.

Carrier-recombination losses in the base that are a fixed percentage of total current account for the flat portion of the beta versus I_c curve. The more heavily doped the base region background doping level is, the larger this fixed percentage of collector current recombination becomes. This is because there are more minority-carrier recombination sites.

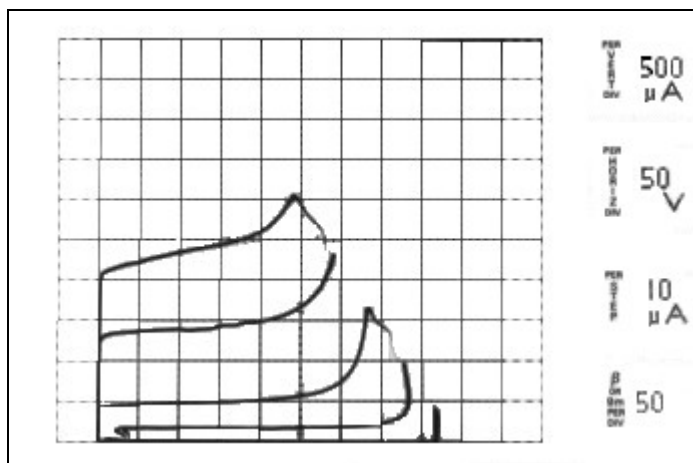


Figure J-17. CE collector characteristic curves showing pronounced low current beta rolloff [74]

Figure J-17 shows a curve tracer display of low-current beta rolloff. The vertical axis is I_c @ 10 $\mu A/\text{div}$ and the horizontal axis is V_{ce} @ 50 volts/div. How was it possible to capture this effect? Device selection, curve tracer settings, or some other neat trick?

This picture was taken off of the display of a Tektronix 576 [74] curve tracer. The curves are generated by a stepped series of forced, fixed base current and a swept collector voltage. The resulting collector current is displayed in a series of curves. Notice how the effective β increases as the collector current level increases from about the 5 μA level to the 45 μA level.

Getting the display to show the low current beta rolloff effect took some manipulation with the curve tracer settings. But the major reason for being able to illustrate the effect is the selection of the device. The device in Figure J-17 shows a very high amount of low current beta rolloff. The BJT had a very high level of fixed losses in the emitter-base space-charge region. A number of processing quality control issues caused carrier recombination sites to go up, including:

- Lattice stresses, damage, and contaminants.
- Hot carrier site injection under the oxide and other effects of reverse biasing the E-B junction.
- Recombination sites are particularly sensitive to surface contaminants because the E-B space charge region meets the surface of a BJT.

As well, a number of other effects can be seen in a poorly processed device. Especially after life test, as in the above case of a contaminated lot. Among these effects are breakdown voltages that change (push) with applied voltage and surface inversion (channeling) across the E-B junction. Observing these effects and other BJT phenomena is discussed more fully in [74].

Interestingly, the semiconductor process that Bardeen, Brattain and Shockley at Bell Labs had available in 1948 prevented them from first finding a surface FET. The surface FET is what they were originally searching for. A high level of contaminants was already inverting their purported surface-field-effect transistor when they stumbled across the BJT effect and recognized it for what it was. They had set out to observe surface inversion on a semiconductor to attempt to build a useful solid-state switching device. They then realized that they were observing minority-carriers injected from a region of p polarity drifting across a narrow gap of n material to a collecting region of p material, and that a bias voltage on the gap material could control this action.

For more on the discovery and theory of the BJT, see [110, 111].

J.8.2.4 Computing Collector Saturation Voltage

Saturation can occur when a transistor is driven very hard. High current through the collector's resistance in the external circuit will cause the voltage at the collector to drop very low, causing the collector-base junction to switch from reverse to forward bias. At this point, the voltage V_{ec} becomes smaller than the voltage V_{eb} . In Figure J-10, the saturation region is seen as a nearly vertical current-voltage line at the left edge of the transistor's characteristic curves. The following equation is from [38].

$$V_{ce(sat)} = \pm \left\{ \frac{k_b T}{q} \ln \frac{\alpha_r [1 - I_c / h_{FE} I_b]}{1 + \frac{I_c (1 - \alpha_r)}{I_b}} + |I_e r_{se}| + |I_c r_{sc}| \right\} \quad (J-12)$$

Where:

α_r is the reverse base transport factor

r_{se} is the emitter saturation resistance, close to the emitter bulk resistance and is usually very small.

r_{sc} is the collector saturation resistance, close to the collector bulk resistance.

Computing the Early Effect Voltage

Another example of structure-based parameter computation is computing Early effect. The Early effect, or base-width modulation, is named after Dr. Jim Early, who explained it. It is an extension, or refinement, to the basic model.

In a bipolar transistor, as the collector-base depletion region widens, some of the spreading will be into the base, causing it to narrow. The spreading will be greater with a lightly doped base. The narrowing will be proportionally greater when the base is narrow to begin with. This narrowing of the base increases the effective β . For a pnp transistor with a linearly-graded collector-base junction, we have [47, 53, 63]:

$$\frac{\partial h_{FE}}{\partial V_{CB}} = - \frac{\left[\frac{W_B}{L_{pb}} + \frac{N_{DB} D_{ne}}{D_{pb} N_{AE} L_{ne}} + \frac{W_{EB} N_{DB} \ell}{2 n_i \tau_o D_{pb}} \right] V_{CB}}{\left[\frac{W_B}{2 L_{pb}^2} + \frac{N_{DB} D_{ne}}{D_{pb} N_{AE} L_{ne}} + \frac{W_{EB} N_{DB} \ell}{2 n_i \tau_o D_{pb}} \right]^2 \left(\frac{1}{q} \epsilon_s \epsilon_o \right)^{1/3} 3 V_{CB}^{4/3}} \quad (J-21)$$

The Early Voltage, a mathematical construct, is defined as:

$$V_{AF} \equiv \left[\frac{1}{W_o} * \frac{\partial W}{\partial V_{BC}} \right]^{-1} \quad (\text{J-22})$$

On an I-V curve such as Figure J-10, the Early voltage can be estimated by extrapolating the linear slopes of the I-V curves to a common point. For more on measuring Early effect, see [63].

The Early Voltage we have just computed from structure in equation (J-22) is the VAF in Table J-7.

J.8.2.5 Computing Collector Breakdown Voltage

Important properties of a transistor's suitability for use include others than those for modeling its behavior as an amplifier or as a switch. There are additional issues of power handling capability, breakdown voltages, temperature rise and its effects, aging and wearout mechanisms, internal noise and the like. One such parameter is BVcbo.

By definition BVcbo is reverse biased collector to base breakdown voltage with the emitter open-circuited. For computing BVcbo for a pnp transistor we [35], [38], have:

$$BV_{CBO} = \epsilon_0 \epsilon_R (E_{crit})^2 / 2qN_{ac} \quad (\text{J-15})$$

N_{ac} is the concentration of acceptor dopants in the collector region.

E_{crit} is the critical electric-field value where avalanche breakdown occurs. Its value relates to the binding energy of an outer electron in an atom being struck by a leakage electron in the collector-base space-charge region. Leakage electrons arise randomly from thermal energy jumping them to the conduction band. There the applied reverse-bias field accelerates them. If they acquire enough energy on their mean free path, they will knock an additional electron free when they strike a lattice or dopant atom. Avalanche multiplication of leakage current then occurs and the junction is said to break down.

A number of mechanisms can cause BVcbo to be lower than the above value. These are reach through, punch through, surface and corner-limited breakdown.

Reach through limited breakdown:

When the collector depletion region on an epitaxial transistor reaches the heavily doped substrate it essentially stops spreading and the applied electric-field strength grows rapidly across the depleted region. Then:

$$BV_{cbo} = E_{crit} * W_{epi} - \frac{qN_{ac}(W_{epi})^2}{2\epsilon} \quad (J-16)$$

where

W_{epi} is the width of the epitaxial layer

Punch through limited breakdown:

When the collector depletion region spreads into the base in a lightly doped base it may eventually reach the base-emitter junction. This has the effect of shorting out the base and turning on the transistor. Then:

$$BV_{cbo} = V_{pt} + BV_{ebo} \quad (J-17)$$

where

V_{pt} is the voltage across the collector-base when this happens.

Surface limited breakdown:

If the collector depletion region at the die surface reaches the edge of the die it encounters a virtually unlimited supply of leakage electrons because of the low binding energy there.

Corner limited breakdown:

The curvature of the collector-base diffusion well causes the shape of the depletion region to be curved as well. This tends to concentrate the field at that corner. Thus, E_{crit} is reached sooner.

J.8.2.6 BJT SPICE Equations

As with the diode, the SPICE bipolar transistor equations and associated parameters are based on the device physics. The default SPICE parameters are for an ideal small-signal BJT having infinite bandwidth.

Charge Equations

$$Q1 = 1/[1 - (VBC / VAF) - (VBE / VAR)] \quad (J-27)$$

$$Q2 = (IS / IKF) * (e^{(VBE / NF * VT)} - 1) + (IS / IKR) * (e^{(VBC / NR * VT)} - 1) \quad (J-28)$$

$$QB = (1/2) * Q1 * (1 + \sqrt{(1 + 4 * Q2)}) \quad (J-29)$$

Base Current

$$\begin{aligned} IB = & (IS / BF) * (e^{(VBE / NF * VT)} - 1) + (ISE) * (e^{(VBE / NE * VT)} - 1) \\ & + (IS / BR) * (e^{(VBC / NR * VT)} - 1) + (ISC) * (e^{(VBC / NC * VT)} - 1) \end{aligned} \quad (J-30)$$

Collector Current

$$\begin{aligned} Ic = & (IS / QB) * [e^{(VBE / NF * VT)} - e^{(VBC / NR * VT)}] - (IS / BR) * (e^{(VBC / NR * VT)} - 1) \\ & - (ISC) * (e^{(VBC / NC * VT)} - 1) \end{aligned} \quad (J-31)$$

Base Resistance

When RBM is specified

$$RBB = RBM + (RB - RBM) / QB \quad (J-32)$$

When RBM and IRB are both specified

(low-current beta rolloff)

$$Z = \{[-1 + \sqrt{1 + (144 * IB / \pi^2 * IRB)}] / (24 * \pi^2 * \sqrt{IB / IRB})\} \quad (J-33)$$

$$RBB = 3 * (RB - RBM) * [(TAN (Z) - Z) / (Z * TAN (Z)^2)] \quad (J-34)$$

Junction Capacitances
(stored charge)

$$TFF = TF * \{1 + XTF * [(IF^2 / (IF + ITF)^2) * e^{(VBC / 1.44 * VTF)}]\} \quad (J-35)$$

$$IF = IS * (e^{(VBE / NF * VT)} - 1) \quad (J-36)$$

$$CBE = TFF * (IS / (QB * VT * NF)) * e^{(VBC / (NF * VT))} + CJE / (1 - (VBE / VJE))^{MJE} \quad (J-37)$$

$$CBC = TR * (IS / (VT * NR)) * e^{(VBC / (NR * VT))} + CJC / (1 - (VBC / VJC))^{MJC} \quad (J-38)$$

$$CSS = CJC / (1 - (VCS / VJS))^{MJS} \quad (J-39)$$

Forward Biased Capacitances
(diffusion capacitances)
All capacitances of the form:

$$CO / (1 - V / \phi)^M \quad (J-40)$$

Revert to the form:

$$CD = CO / (1 - FC)^{(1+M)} * \{1 - FC(1 + M) + M * (V / \phi)\} \quad (J-41)$$

when:

$V > FC * \phi$ and

FC taken as 0 for CSS

Gain-Bandwidth

$$Ft = (1 / (2 * \pi)) * \{1 / [TF * QB + (VT / IC) * [CJE(1 - (VBE / VJE))^{MJE} + CJC(1 - (VBC / VJC))^{MJC}]]\} \quad (J-42)$$

If the BJT is operated below IKF, the high-current injection knee, and with $V_{CB} \gg V_{CEsat}$, then F_t simplifies to:

$$F_t' = 1/(2 * \pi * TF) \quad (J-43)$$

Turn-Off Time

(TR is related to TS: storage time)

$$TR = (TS / BR) / [\ln((IB1 + IB2) / ((IC / BF) + IB2))] \quad (J-44)$$

where:

TS is the measured storage time

IC1 is the initial collector current when the transistor is saturated

IB1 is the forward turn-on base current

IB2 is the reverse turn-off base current

Bulk Resistor Noise

Resistors RC, RB, and RE are each modeled with an equivalent noise current of:

$$i^2 = 4 * K * T * (B / R) \quad (J-45)$$

where:

i is the spectral noise: Amps/ $\sqrt{\text{Hz}}$

B is the bandwidth in Hz

Shot and Flicker Noise

$$(i')^2 = (2 * q * I * B + KF * B * (I)^{AF}) / F \quad (J-46)$$

where:

i' is the spectral noise: Amps/ $\sqrt{\text{Hz}}$

F is the analysis frequency

Effect of Temperature on Parameters

$$IS @ T = IS_{NOM} * (T / T_{NOM})^{(XTI / NF)} * e^{(EG / (NF * VT))((T - T_{NOM}) / T_{NOM})} \quad (J-47)$$

$$ISE @ T = ISE_{NOM} * (T / T_{NOM})^{((XTI - XTB) / NE)} * e^{(EG / (NE * VT))((T - T_{NOM}) / T_{NOM})} \quad (J-48)$$

$$ISC @ T = ISC_{NOM} * (T / T_{NOM})^{((XTI - XTB) / NC)} * e^{(EG / (NC * VT))((T - T_{NOM}) / T_{NOM})} \quad (J-49)$$

$$BF @ T = BF * (T / T_{NOM})^{XTB} \quad (J-50)$$

$$BR @ T = BR * (T / T_{NOM})^{XTB} \quad (J-51)$$

$$VJE @ T = VJE * (T / T_{NOM}) - 2 * VT * [1.5 * \ln(T / T_{NOM}) - EG / (2 * VT - 1.115 * VTO)] \quad (J-52)$$

$$VJE @ T = VJE * (T / T_{NOM}) - 2 * VT * [1.5 * \ln(T / T_{NOM}) - EG / (2 * VT - 1.115 * VTO)] \quad (J-53)$$

$$VJC @ T = VJC * (T / T_{NOM}) - 2 * VT * [1.5 * \ln(T / T_{NOM}) - EG / (2 * VT - 1.115 * VTO)] \quad (J-54)$$

J.8.2.7 Comparison of SPICE Properties for Several BJT Devices

Table J-8 compares some selected non-defaulted SPICE parameters for several discrete BJT transistors, both npn and pnp. As a general rule, npn transistors have higher gain, since electrons have higher mobility in the base region than holes do. The difference in the SPICE parameters for different devices illustrates the importance of having the correct parameters.

All the SPICE parameters for current, such as IS have positive signs. The simulator equations change signs as necessary between npn and pnp models, so that current and junction voltages maintain appropriate physical polarities in all operating regions.

Table J-8. Small-signal general-purpose amplifier and switches

Name	2N3904 (nnp)	2N4400 (nnp)	2N4410 (nnp)	MPSA05 (nnp)	2N4402 (pnp)
IS	6.734f	26.03f	5.911f	8.324f	.6506f
BF	416.4	7756	413.6	12160	108
NF	Default = 1				
VA	74.03	90.7	62.37	100	115.7
IKF	66.78m	239.7m	12.6m	109.6m	1115m
ISE	6.734f	26.7f	5.911f	73.27f	146.9f
NE	1.259	1.204	1.278	1.368	1.86
BR	0.7371	1.06	1.361	11.1	3.83
NR	Default = 1				

Name	2N3904 (npn)	2N4400 (npn)	2N4410 (npn)	MPSA05 (npn)	2N4402 (pnp)
VAR	Default = infinity				
IKR	0	0	0	0	0
ISC	0	0	0	0	0
NC	2	2	2	2	2
RB	10	10	10	10	10
IRB	Default = infinity				
RBM	Default = 10				
RE	Default = 0				
RC	1	.5	1.61	.25	.715
CJE	4.493p	24.07p	4.973p	55.61p	19.82p
VJE	0.75	0.75	0.75	0.75	0.75
MJE	0.2593	0.3641	0.4146	0.3834	0.3357
TF	301.2p	573.2p	818.4p	516.1p	761.3p
XTF	2	0	7	6	1.7
VTF	4	0	4	4	5
ITF	0.4	0	0.35	0.5	0.65
PTF	Default = 0				
CJC	3.638p	11.01p	4.017p	18.36p	14.76p
VJC	0.75	0.75	0.75	0.75	0.75
MJC	0.3085	0.3763	0.3174	0.3843	0.5383
XCJC	Default = 1				
TR	239.5n	244n	4.749n	72.15n	115.7n
CJS	Default = 0				
VJS	Default = .75				
MJS	Default = 0				
XTB	1.5	1.5	1.5	1.5	1.5
EG	1.11	1.11	1.11	1.11	1.11
XTI	3	3	3	3	3
KF	Default = 0				
AF	Default = 1				
FC	0.5	0.5	0.5	0.5	0.5

Table J-8 shows clearly that device construction affects SPICE parameter values. Parameters like mid-current DC current gain, β ; low and high current β range, and linearity of β with collector voltage interrelate with each other and with other SPICE related behavior. For the definitions of the parameters in Table J-8, refer to Table J-7 and the associated discussion in the text.

In Tables 6-3, 6-4, and 7-2, we look at this same set of devices and see that as devices grow larger and more rugged (able to handle larger voltages, currents, and power), they become slower in switching speed and bandwidth capabilities. SPICE is used to compute transistor behavior as an amplifier or as a switch. But SPICE is not designed to handle extreme conditions such as self-heating or reversed-biased second breakdown. Voltage, current and power handling capabilities are outside of SPICE's focus. For instance,

asking for a device with a particular gain-bandwidth capability has consequences for the magnitude of voltage-standoff capability. For example, a video amplifier chip, used to drive the video gun of a CRT, peaks out at around 100MHz gain-bandwidth and 300V BVceo. Attempts to modify the device design to achieve significantly better gain bandwidth will succeed only by giving up some breakdown voltage capability.

Almost all the shifts in SPICE parameter behavior and power handling behavior can be predicted and studied from TCAD formulas. There is a level of very sophisticated device design techniques that extend device capabilities. For instance, there are device construction techniques that enhance high-current β holdup, voltage standoff, and many other performance factors. These techniques shape electric fields and depletion regions in the silicon, the steepness of doping gradients, and other factors. The discussions of these techniques are a subject for semiconductor device designers and are not relevant to a book on circuit design.

For deep sub-micron CMOS, tradeoff issues would typically involve geometry size, switching speed, current handling, current electromigration resistance, threshold and noise margins, and ESD ruggedness among others.

J.8.3 The MOSFET Transistor

J.8.3.1 Introduction

There are literally dozens of SPICE models for MOSFET transistors. These models cannot be covered completely here. Many additional factors have entered into device modeling, up to and including quantum effects. Quantum effects result from the nature of the extremely small device dimensions in the lateral surface direction. In the past, horizontal dimensions were very much larger than vertical dimensions. Now horizontal dimensions are comparable or even much smaller.

Two excellent resources for studying MOSFET modeling are:

- The Berkeley models:
<http://www-device.eecs.berkeley.edu/~bsim3/get.html> [117]
- The Enz, Krummenacher, and Vittoz EKV (Enz, et al., 1995) model:
<http://legwww.epfl.ch/ekv/> [35]
- The Applied Computational Research Society site:
<http://www.cr.org/index.html>

BSIM3 and BSIM4 models tend to be based more on curve fitting and binning, while the EKV models are based on physical conservation laws (charge, energy, and fields at boundaries). The EKV models were designed to address MOSFETs operating in low-to-moderate channel inversion, which is characteristic of low-voltage and small-signal integrated circuits. BSIM models, on the other hand, were designed to model digital MOSFETs switching from cutoff to strong inversion.

J.8.3.2 MOSFET Equivalent Circuit

The BSIM MOSFET model in SPICE is based on the equivalent circuit shown in Figure J-18 and corresponds to SPICE2 from UC Berkeley. All of the capacitors and current sources are bias-dependent; the default values of the capacitors are 0.0, which represents an infinite bandwidth.

The SPICE model does not account for any source and drain transit time; this mainly affects accuracy for high-voltage switching MOSFETs. The model assumes that the gate-oxide layer and source/substrate and drain/substrate junctions do not go into breakdown. These additional physical effects can be addressed by embedding a MOSFET inside a larger subcircuit that models these effects.

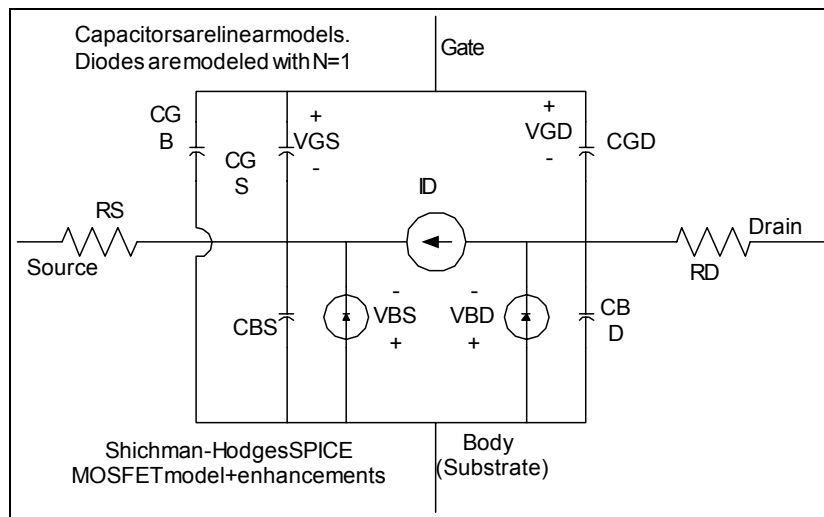


Figure J-18. MOSFET equivalent circuit [84]

J.8.3.3 SPICE MOSFET Parameters

The MOSFET SPICE parameters and device equations are covered in detail in “Appendix J, Device Physics.” Some selected parameters are shown in Table J-9 for illustration. Equations (J-23) to (J-27) are a sample of the SPICE MOSFET equations that use these parameters. For a complete set of MOSFET SPICE2 parameters refer to “Appendix J, Device Physics.” Table J-9 is based on SPICE2 [152]. Berkeley has released several newer MOSFET models, from MOS1 to BSIM4. Most SPICE versions also support the EKV MOSFET model (which came from a group in Europe).

Table J-9. SPICE2 MOSFET model parameters [84] from UC Berkeley

Name	Parameter	Units	Default Value
LEVEL	Model index		1
VTO	Zero bias threshold	V	0
KP	Transconductance	A/V ²	2e-5
GAMMA	Bulk threshold parameter	V ^{1/2}	0
PHI	Surface potential	V	.6
LAMBDA	Channel length modulation MOS1 & MOS2 only	1/V	0
RD	Drain ohmic resistance	Ohms	0
RS	Source ohmic resistance	Ohms	0
CBD	Zero bias B-D junction capacitance	F	0
CBS	Zero bias B-S junction capacitance	F	0
IS	Bulk junction saturation current	A	1e-14
PB	Bulk junction potential	V	0.8
CGSO	Gate-Source overlap capacitance	F/m	0
CGDO	Gate-Drain overlap capacitance	F/m	0
CGBO	Gate-Bulk overlap capacitance	F/m	0
RSH	Drain & Source diffusion sheet resistance	Ω/sq	0
CJ	Zero bias bulk junction bottom capacitance	F/m ²	0
MJ	Bulk junction bottom grading coefficient		0.5
CJSW	Zero bias bulk junction sidewall capacitance	F/m	0
MJSW	Bulk junction sidewall grading coefficient		0.33
JS	Bulk junction saturation current density	A/m ²	0
TOX	Oxide thickness	m	1e-7
NSUB	Substrate doping	cm ⁻³	0
NSS	Surface state density	cm ⁻²	0
NFS	Fast surface state density	cm ⁻²	0
TPG	Type of gate material: 1 = opposite of substrate, -1 = same as substrate, 0 = Al gate		1
XJ	Metallurgical junction depth	m	0
LD	Lateral diffusion	m	0
UO	Surface mobility	cm/V-s	600
UCRIT	Critical field for mobility degradation MOS2	V/cm	1e+4

Name	Parameter	Units	Default Value
	only		
UEXP	Critical field exponent for mobility degradation MOS2 only		0
UTRA	Transverse field coefficient in mobility degradation MOS2 only		0
VMAX	Maximum drift velocity of carriers	m/sec	0
NEFF	Total channel charge coefficient (fixed & mobile) MOS2 only		1
XQC	Thin oxide capacitance flag and coefficient of channel charge attributable to drain (0-.5)		1
KF	Flicker noise coefficient		0
AF	Flicker noise exponent		1
FC	Coefficient for forward bias depletion capacitance		0.5
DELTA	Width effect on threshold voltage, MOS2 and MOS3		0
THETA	Mobility modulation, MOS3 only	1/V	0
ETA	Static feedback, MOS3 only		0
KAPPA	Saturation field factor, MOS3 only		0.2

J.8.3.4 MOSFET SPICE Equations

A few MOSFET model equations (J-23) through (J-26) are shown for illustration. These equations are level 1 and level 2 with terms for gate modulation specifically included because this effect will be referred to later. Additional equations, governing such things as MOS junction capacitance, can be found in the references [10, 11, 21, 22, 28, 32, 35,38, 40, 42, 47, 63, 68, 77, 84, 86, 90, 97, 98, 100, 109, 117, 118, 121, 127, 132, 133, 140, 152].

For: Forward Region, $V_{DS} > 0$

$$I_D = 0 \quad (3-23)$$

For: $V_{GS} - V_{TO} < 0$

$$I_D = (KP/2) * (W/L) * (V_{GS} - V_{TE})^2 \quad (3-24)$$

For: $0 < V_{GS} - V_{TO} < V_{DS}$

$$I_D = (K_P/2) * (W/L) * V_{DS} * (2 * (V_{GS} - V_{TE}) - V_{DS}) * (1 + LAMBDA * V_{DS}) \quad (3-25)$$

For: $0 < V_{DS} < V_{GS} - V_{TO}$,
where:

$$V_{TE} = V_{TO} + GAMMA * (\sqrt{2PHI - V_{BS}} - \sqrt{2PHI}) \quad (3-26)$$

J.9 MODELING PACKAGING INTERCONNECTIONS

Related to modeling the silicon die is modeling the package and interconnections on and around the chip. The circuit designer needs a model of the whole IC, including interconnections, bond wires, package, and pins. SPICE models in the public domain usually include none of this information. On-die metalization interconnections modeling may be included in some EDA packages and is certainly included by silicon designers as part of their validation and verification process. Today's deep sub-micron switching speeds are tens of picoseconds or less in switching speed edge rates. Signal Integrity, crosstalk, Power Integrity, and EMI/EMC concerns have migrated into the design of the silicon and its packaging. The challenge to the silicon designer and packaging engineer is not lessened by the fact that they do not control the power supplies and power returns—the circuit designer does.

While devices have been shrinking, interconnection technology has also changed. For example:

- Metal and dielectric layer thicknesses have changed. Some of the latest deep-sub-micron technology is working with oxide thicknesses only three atoms wide.
- Horizontal feature size has shrunk dramatically.
- Metal width-to-height ratios have dropped from 3:1 to about 1:3.
- The number of metal layers on a chip has increased from 2 or 3 to over 8. One consequence is that capacitance between adjacent wires is now dominant over trace-to-ground capacitance.

J.9.1 Wavelengths Have Shrunk: Interconnections Affect Everything

Package and board design technology have advanced as well. Packages are now being designed with controlled impedance, similar to how high-speed boards have been designed for years. Increasing via density has resulted in more porous ground and power planes, making it more difficult to predict impedance. These changes in package technology have led to the use of 2D and even 3D field solvers to model interconnections at the IC package, and board level. The models are commonly expressed as lumped SPICE subcircuits, RLGC matrices, or S-Parameters.

Field solvers were once rarely used in semiconductor device analysis. They had been mainly used to extract parameters for PCB-level transmission lines, connectors, and cables. For PCB level use, the extraction of parasitics on IC package pins and mutual-coupling effects between pins are sufficient for SI needs.

Now however, with device speeds and edge rates pushing frequency content into the tens of GHz range, field solvers are beginning to see more use. Field solvers are now in widespread use for high-speed ICs. 3D field solvers [113] are mostly used, since there is no ground plane in the IC package itself.

But what about the question of possible EMI radiation and conducted emissions from an IC package? The problem or radiation from IC packages is beginning to receive some attention. The trouble is, little is known about what the issues are. Little has been published on this subject, and many of those doing work in the field treat it as proprietary information.

We do know that IC packages can radiate. Plots of near-field simulations, showing the same board with and without the IC package radiation accounted for, are available. That work was done in close collaboration with one of the EDA supplier's customers. The plots are significantly different. The software provider stated that good correlation between EM-scan results and EMI simulation is not achievable without accounting for the ICs. But the work and the customer's name are proprietary.

How should we model the issues involved? Is the radiation coming from the loop formed by voltage supply rings? Or from via currents that do not have canceling image currents on the power planes because they are perpendicular to the image planes? We suspect that the major effect is from the vias. Or is it due to conducted emissions onto the PCB interconnections? Or some other issue? Packaging engineers seem shocked that anybody thinks their packages radiate. Or else, they see it as entirely the responsibility of the user to figure such things out, because it was the users who determined where to locate the image planes.

Another issue to address in EMI simulation is the ability to analyze the whole problem. EMI software providers have made great strides in improving their products. However, the authors are not aware of any software vendor offering a product that simulates EMI and Signal Integrity issues from the chip to far-field regulatory requirements.

All the same, one author [Leventhal, 85] provided modeling support for a client who needed to simulate near field EMI, to apply source-suppression techniques to pass regulatory requirements. The results correlated well to their lab measurements, enabling the application of useful simulation-based source suppression. In this case, adding an enclosure was not acceptable. Thus, an enclosure with its resonance effects and other coupling and loading effects did not enter into the simulations. So, near-field prediction and hot-spot suppression translated directly into passing regulatory requirements. Another effect of making simulation work is realizing that a designer should:

1. Apply good engineering rules-of-thumb to limit the problems that must be solved by simulation.
2. Apply simulation to sort out conflicts between the rules-of-thumb.

J.9.2 Standards for EMI/EMC Design

Industry and profession society standards committees and organizations have long been involved in developing standards for components and models. Table J-10 lists some of these organizations now involved in EMI/EMC issues in modeling.

Table J-10. Web sites of standards organizations involved in modeling package parasitics and EMI effects

Committee	Web address
EIA/IBIS Committee	Home page http://www.eigroup.org/ibis/ Input/Output Buffer Information Specification(s): downloadable http://www.eigroup.org/ibis/specs.htm IBIS Interconnections Model (ICM) Specification: draft proposal Intel is pushing this to be used as the proposed IC package specification http://www.eda.org/pub/ibis/connector/
IEC	International Electrotechnical Commission. International standards and conformity assessment for government, business and society for all electrical, electronic and related technologies. Home page http://www.iec.ch/index.html Integrated Circuit Electrical Model & Cookbook: draft proposal http://www.eigroup.org/ibis/specs.htm
IEEE	Institute of Electrical and Electronics Engineers. Home page http://www.ieee.org/portal/index.jsp EMC Society http://grouper.ieee.org/groups/emc/index.html

Committee	Web address
JEDEC	The JEDEC Solid State Technology Association (Once known as the Joint Electron Device Engineering Council) is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. JEDEC was originally created in 1960 as a joint activity between EIA and NEMA, to cover the standardization of discrete semiconductor devices and later expanded in 1970 to include integrated circuits. Home page http://www.jedec.org
JEITA	Japan Electronics and Information Technologies Industries Association. Formed by the merger of EIAJ and JEIDA of Japan. JEITA's mission is to foster a digital network society for the 21 st century. Among their many activities are the formulation of component and modeling standards for Japan.
CMC	Compact Model Council. The CMC is a group of Semiconductor Vendor companies and EDA Vendor companies that standardizes any compact model formulation that meets the business needs of its member companies. Currently, there is an effort in MOS, Bipolar, and SOI technology processes. Home page http://www.eigroup.org/cmc/

Much remains to be done in the engineering community regarding EMI/EMC simulation. These industry committees are addressing some of the modeling issues involved. The IBIS and IEC Committees are working on model standards for Power Integrity and SSN/SSO. The IEEE EMC Society is getting deeply involved in the modeling and simulation of EMI/EMC.

J.10 SUMMARY

SPICE was developed to simulate device circuit behavior. Over time, the SPICE program became synonymous with SPICE models. SPICE models can be quite complex, containing more than 200 parameters and 60 circuit nodes in a modern, deep sub-micron CMOS device. Deep-sub-micron CMOS devices are usually simulated with the aid of CAE software programs, collectively known as TCAD programs.

SPICE is the best model for understanding how circuit behavior relates to the internal physical construction of devices. SPICE parameters are also used to monitor and control semiconductor processes because of their often-close relationship to structure and chemistry. The device physics parameters that are useful for controlling semiconductor processes do not coincide exactly with the SPICE parameters that are useful for circuit simulation and analysis.

Engineers should understand the precise SPICE model received from a silicon foundry and the assumptions used to derive that model. In addition, sometimes the model contains errors from a circuit analysis point of view and does not run immediately in a particular simulator.

Not all SPICE parameters have direct physical meaning. Some parameters are purely curve-fitting properties that must be measured rather than be derived from structure.

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